

## Methods for Controlling Autonomous DC Systemson the Basis of Switching by Capacitors

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### Abstract

The article demonstrates methods for constructing pulse-amplitude (PAM) and pulse-width (PWM) controlled DC systems on the basis of switched-capacitor structures. Represented is the optimal structure of the system of DC electrical power interchanges (SEI), which excludes the use of additional elements. Proposed are the algorithms for controlling SEI transistor keys and their regulating characteristics. Studied are the features of their work and obtained are the equations for calculating the power circuit parameters.

**Keywords:** bidirectional DC regulators, system of DC electrical power interchanges, pulse amplitude and pulse width modulated control

### I. Introduction

As it is known, a frequency converter (FC) is an electronic device that converts AC electric power of one frequency to AC electric power of another frequency.

Currently, in the autonomous systems there are used two types of frequency converters (FC) with an intermediate DC link and direct frequency converters (DFCs), designed on the basis of power semiconductor devices. Such converters, if compared to the electromechanical ones, have superior performance specifications (1).

FC can be used for both step-up and to decreasing frequency of the current generated by independent power supply sources. Regardless of the conditions provided, they can perform two functions: stabilize current frequency and voltage. Furthermore, these two functions are performed by the FC control system independently (1).

Converters with an intermediate DC link, due to the double-conversion of electric power (they convert AC to DC and then DC to AC of the required frequency) possess low efficiency values, extra weight and dimensions in comparison with DFCs.

Modern power supply of autonomous systems is often made from several DC sources with differently time-varying voltages. As a result, there arises a problem of controlling the fluxes of electrical power when they are combined into a single system of DC electrical power interchanges (SEI). One of the simplest solutions is the use of bi-directional DC-DC converters with a variable conversion coefficient. The basic requirements of this installation include high efficiency, wide range of adjustment, low harmonic factor of the input and output currents, and linearity of regulating characteristics. Power circuit schematic (PC) is a simplest bilevel SEI based on the bidirectional converter module (BCM) (Figure 1) (Zotov, 2011).

Oscillatory forming circuits, which consist of capacitance  $C_1$  and inductance  $L_1$ , provide for switching all transistor keys at a time point when the currents passing through them are equal to zero (soft switching mode). Thus, losses in transistor keys at switching are minimized.

Reactors  $L_1$  and capacitors  $C_1$  form series-oscillatory circuits that provide for switching all transistor keys at the time points when the currents passing through them are equal to zero (soft switching mode). As a result, the switching losses in the transistor keys are minimized, which has a positive effect on efficiency. However, a

disadvantage of such a system is the lack of electric power adjustment, which  $P_1$  and  $P_2$  are interchanged by low-voltage  $E_1$  and high-voltage  $E_2$  power supplies during SEI operation in both directions (Resonant DC-DC converters on the basis of switched-capacitor structures for autonomous power supply systems. "Radio industry", 2012, Vol. 1: 103-113; Zotov and Zinoviev, 2014; Evseev and Yurov, 2011; Golubkina, I.V. et al. 2011; Gorskii and Sysenko, 2009; 7. Boroday et al., 2008).

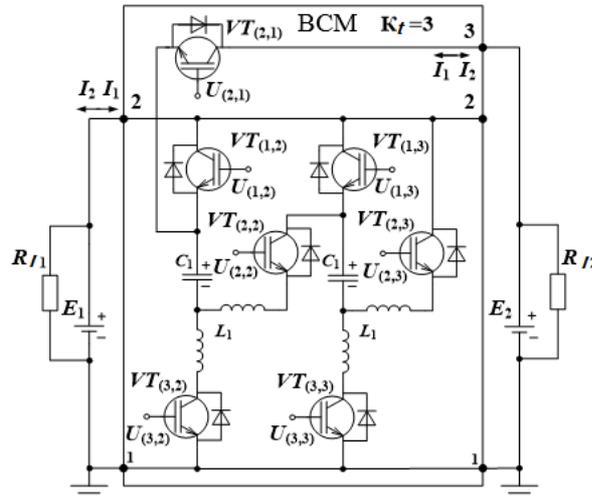


Figure 1. Power circuit schematic of a bilevel SEI on the basis of BCM

Regulation of the system given is impossible without additional diodes across the inductance  $L_1$ . The absence of regulation is necessary, as the situation may arise when the value of voltage separation  $|(N + 1) \cdot E_1 - E_2|$  may reach quite a high level. This will lead to a significant reduction in plant efficiency and, in addition, may cause a substantial increase in currents through the elements of power circuit being above the calculated ones, which will result in their failure.

The simplest solution to this problem is to use a PWM regulator at the BCM input and output. The main advantage is a high efficiency level. The disadvantage is a high harmonics factor value of DC source being a donor.

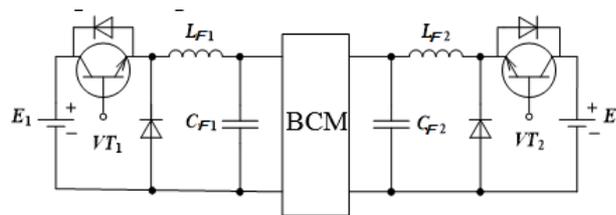


Figure 2. Block-diagram of SEI with PWM regulators

## 2. Regulated SEI Structure

The basic requirements for a regulated SEI is a high level of efficiency and low values of harmonic factors of the input and output currents. Therefore follows the solution of the problem, which is to impose functions of regulating elements on the transistor keys already existing in SEI (Figure 3). This offers new opportunities for regulation performance by a variety of methods.

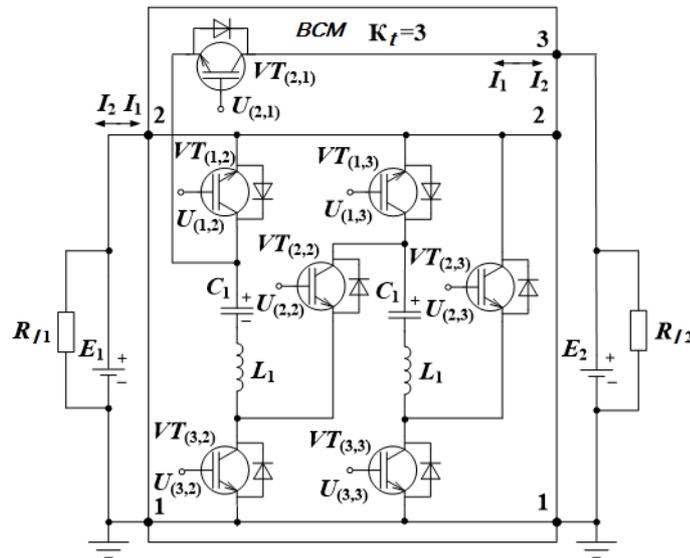


Figure 3. Power circuit schematic of a regulated SEI

### 3. Regulated SEI (PAM)

The most obvious regulation method is based on the SEI pulse amplitude modulation (PAM).

It is carried out by changing the active resistance  $R_T$  of transistor keys  $VT(i, j)$  included into the BCM power circuit. In this case it is necessary to consider the behaviour of the SEI (PAM) efficiency –  $\eta(R_T)$  and the power level in both directions  $P_1(R_T)$ ,  $P_2(R_T)$  from the regulating parameter  $R_T$ .

At SEI operation in the mode of continuous electric power transmission, and this is possible if the system is controlled by charging and discharging BCM keys. The system operates as an ideal current transformer. Current conversion coefficients depend only on the number of capacitances involved in the conversion of  $N$  and are determined by

$$K_{t(i)} = \frac{I_{1(av)}}{I_{2(av)}} = N + 1 \text{ и } K_{t(i)} = \frac{I_{2(av)}}{I_{1(av)}} = \frac{1}{N+1} \quad (1)$$

Consequently, the efficiency of SEI (PAM)

$$\eta_{dir} = \frac{P_2}{P_1} = \frac{E_2 \cdot I_{2(av)}}{E_1 \cdot I_{1(av)}} = \frac{E_2}{E_1} \cdot \frac{1}{N + 1} \quad (2) \quad \eta_{rev} = \frac{P_2}{P_1} = \frac{E_1 \cdot I_{1(av)}}{E_2 \cdot I_{1(av)}} = \frac{E_1}{E_2} \cdot (N + 1) \quad (3)$$

At specified values  $E_1$  and  $E_2$ , the adjustment of output power  $P_1(R_T)$ ,  $P_2(R_T)$  is carried out at a constant efficiency level, and the boundary conditions of permitted deviation  $E_{1max}$  and  $E_{2max}$ , at which the adjustment is allowed, are determined through the target values of the minimum efficiency  $\eta_{up min}$  and  $\eta_{op min}$  during the SEI operation. It follows from the expressions (2) and (3) that

$$E_2 \cdot \frac{1}{N+1} < E_{1max} < \frac{E_2}{\eta_{dir min}} \cdot \frac{1}{N+1} \quad (4)$$

$$E_1 \cdot (N + 1) < E_{2max} < \frac{E_1}{\eta_{rev min}} \cdot (N + 1) \quad (5)$$

When using this method, the inductances  $L_1$  may be excluded from power circuit, but it should be noted that the harmonic factors of the input and output currents are meanwhile strongly distorted. In addition, there comes a substantial reduction of the regulated power level and a significant increase in the amplitude of current pulses through the transistor keys of SEI power circuit.

In this case, control matrices of the corresponding transistor keys  $VT(i, j)$  being as a part of BCM will take the following form

$$\begin{vmatrix} U_{(1,1)} & U_{(1,2)} & U_{(1,3)} \\ U_{(2,1)} & U_{(2,2)} & U_{(2,3)} \\ U_{(3,1)} & U_{(3,2)} & U_{(3,3)} \end{vmatrix} = \begin{vmatrix} - & 0 & 0 \\ 0 & \bar{X} & \bar{X} \\ - & X & X \end{vmatrix}, \begin{vmatrix} - & X & X \\ \bar{X} & 0 & 0 \\ - & 0 & 0 \end{vmatrix}.$$

Where X – is a periodic sequence of SEI power circuit control pulses;

$\bar{X}$  - is an inverted control signal X;

0- is a blocking signal of a corresponding transistor key.

Adjustment characteristics of SEI (PAM) in the forward and reverse directions of work (Figure 4 and Figure 5).

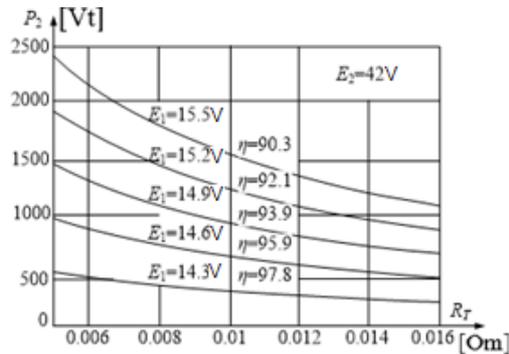


Figure 4. Adjustment characteristics of SEI (PAM) in the forward direction

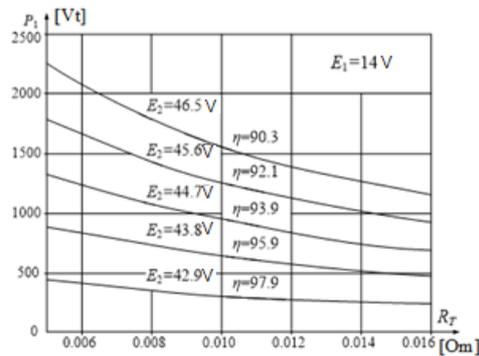


Figure 5. Adjustment characteristics of SEI (PAM) in the reverse direction

Rated values of the SEI power circuit values are determined based on the maximum power values in the forward  $P_{2(max)}$  and reverse  $P_{1(max)}$  directions. Then the voltage values of the input and output sources at SEI operation in both forward and reverse directions  $E_{1(\rightarrow)}, E_{1(\leftarrow)}, E_{2(\rightarrow)}, E_{2(\leftarrow)}$  are determined from the following equations

The values of capacitances and inductance of SEI power circuit are determined by the following expressions

$$\frac{E_{2(\leftarrow)}}{P_{2(max)}} = \frac{E_{2(\rightarrow)}}{P_{1(max)}} = (N + 1) \tag{6}$$

$$C_1 = \frac{E_{1(\rightarrow)} \cdot P_{1(max)}}{f_K \cdot \Delta U_{c1} \cdot E_{2(\rightarrow)}} = \frac{E_{1(\leftarrow)} \cdot P_{1(max)}}{f_K \cdot \Delta U_{c1} \cdot (N + 1) \cdot E_{1(\leftarrow)}} \tag{7}$$

$$L_1 = \frac{1 + \sqrt{1 - 4 \cdot \pi^2 \cdot f_K^2 \cdot R_1^2 \cdot C_1^2}}{8 \cdot \pi^2 \cdot f_K^2 \cdot C_1} \tag{8}$$

Where  $\Delta U_{C1}$  – is a permissible value of the voltage ripple on capacitors  $C_1$ ,

$R_1^2$  – is an overall resistance of the transistor keys in low-voltage and high-voltage SEI circuits.

At the coordination of output power  $P_2(R_T)$ , there is a change in ripple value  $\Delta U_C$ . Standard dependences  $\Delta U_C(R_T)$  are shown in Figure 6.

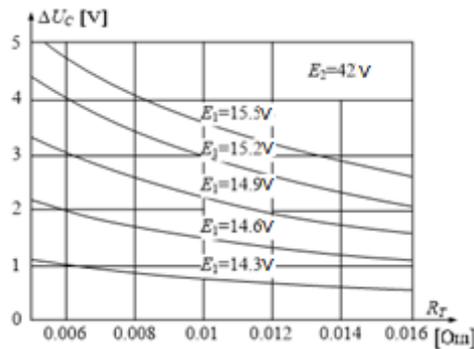


Figure 6. Dependences of the voltage ripple across the BCM capacitors on the resistance of transistor keys

#### 4. Regulated SEI (PWM)

Control over the electric power fluxes in SEI is also possible within the pulse-width modulation (PWM) method (Figure 3). PWM application allows for step-up SEI efficiency level. PC (Fig.3) allows various adjustment methods on the basis of PWM. Adjustment in both directions can be performed using PWM of transistor keys of both low voltage [ $VT_{(1,1)}$ ,  $VT_{(3,1)}$ ], and high-voltage  $VT_{(2,1)}$  BCM circuits.

When adjusting a low-voltage circuit by transistor keys, the PWM in forward direction is carried out through changing a duty factor  $\gamma_{(3,2)}$ ,  $\gamma_{(3,3)}$  of the control pulses  $U_{(3,2)}$ ,  $U_{(3,3)}$  of the transistor keys  $VT_{(3,2)}$ ,  $VT_{(3,3)}$ . At SEI operating in reverse direction, changed are the duty factors  $\gamma_{(1,2)}$ ,  $\gamma_{(1,3)}$  of the control pulses  $U_{(1,2)}$ ,  $U_{(1,3)}$  of the transistor keys  $VT_{(1,2)}$ ,  $VT_{(1,3)}$ . In this case, the control matrices in forward and reverse directions of SEI operation, respectively, have the following form

$$\begin{vmatrix} U_{(1,1)} & U_{(1,2)} & U_{(1,3)} \\ U_{(2,1)} & U_{(2,2)} & U_{(2,3)} \\ U_{(3,1)} & U_{(3,2)} & U_{(3,3)} \end{vmatrix} = \begin{vmatrix} - & 0 & 0 \\ 0 & \overline{X} & \overline{X} \\ - & X(\sim) & X(\sim) \end{vmatrix}, \begin{vmatrix} - & X(\sim) & X(\sim) \\ \overline{X} & 0 & 0 \\ - & 0 & 0 \end{vmatrix}$$

Here  $X(\sim)$  – is a control signal  $X$ , which duty factor is adjustable between 0 to 0.5,  $\overline{X(\sim)}$  - is an inverted control signal  $X(\sim)$ .

If the adjustment is carried out through the transistor keys of a high voltage circuit in the forward direction, then it is realized through the change in duty factor  $\gamma_{(2,3)}$  of the control pulses  $U_{(2,3)}$  of a transistor key  $VT_{(2,3)}$ . At SEI operating in a reverse direction, the adjustment is carried out by changing duty factor  $\gamma_{(2,1)}$  of the control pulses  $U_{(2,1)}$  of the extreme transistor key  $VT_{(2,1)}$ . The change  $\gamma_{(2,1)}$  takes place within the range of 0 to 0.5. The work of the SEI power circuit transistor keys in forward and reverse directions is respectively described by the following control matrices

$$\begin{vmatrix} U_{(1,1)} & U_{(1,2)} & U_{(1,3)} \\ U_{(2,1)} & U_{(2,2)} & U_{(2,3)} \\ U_{(3,1)} & U_{(3,2)} & U_{(3,3)} \end{vmatrix} = \begin{vmatrix} - & 0 & 0 \\ 0 & \overline{X} & \overline{X(\sim)} \\ - & X & X \end{vmatrix}, \begin{vmatrix} - & X & X \\ \overline{X(\sim)} & 0 & 0 \\ - & 0 & 0 \end{vmatrix}$$

There is also possible a combined method of regulation, when adjustment in the forward direction is carried out through the change in duty factor of the control pulses  $U_{(3,2)}$  and  $U_{(3,3)}$  of the transistor keys  $VT_{(3,2)}$ ,  $VT_{(3,3)}$  of a low-voltage circuit, and in the reverse direction it is carried out through the change in duty factor  $\gamma_{(2,1)}$  of the control pulses  $U_{(2,1)}$  of the transistor key  $VT_{(2,1)}$  of a high-voltage circuit. Change in the  $\gamma_{(3,i)}$  and  $\gamma_{(2,1)}$  coefficients also happens within the range of 0 to 0.5.

Control matrices of the combined SEI (PWM) during its operation, respectively, in the forward and reverse directions have the following form

$$\begin{vmatrix} U_{(1,1)} & U_{(1,2)} & U_{(1,3)} \\ U_{(2,1)} & U_{(2,2)} & U_{(2,3)} \\ U_{(3,1)} & U_{(3,2)} & U_{(3,3)} \end{vmatrix} = \begin{vmatrix} - & 0 & 0 \\ 0 & \bar{X} & \bar{X} \\ - & X(\sim) & X(\sim) \end{vmatrix}, \begin{vmatrix} - & X & X \\ \bar{X}(\sim) & 0 & 0 \\ - & 0 & 0 \end{vmatrix}$$

Standard regulating characteristics  $P_2[\gamma_{(3,i)}]$ ,  $P_1[\gamma_{(2,i)}]$  during the operation of SEI (PWM) with a combined control, respectively, in forward and reverse directions are shown in Figure 7 and Figure 8.

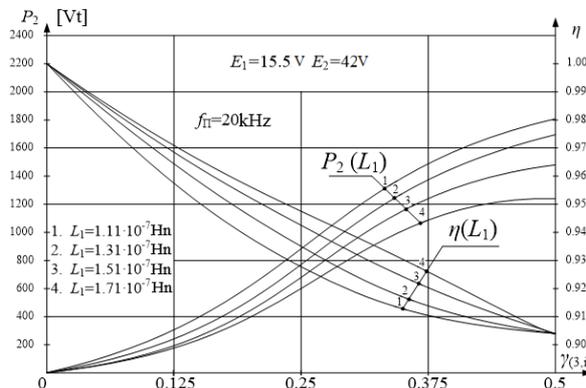


Figure 7. Regulating characteristics of a combined SEI (PWM) in forward direction

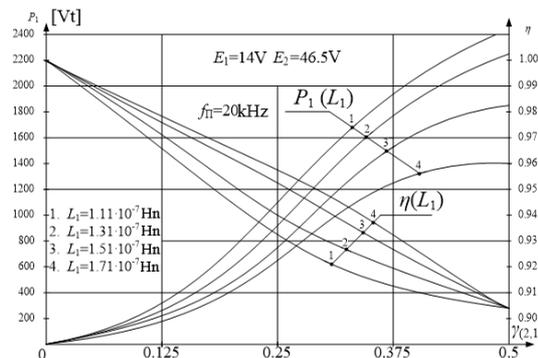


Figure 8. Regulating characteristics of a combined SEI (PWM) in reverse direction

### 5. Multilevel DCRs with a Sectionalized Input Source

Multizone pulse-width DC regulators (DCR) with a sectionalized input source, which distinguishing features are: increased efficiency level and linearity of a regulating characteristic. Block-diagram of a bilevel bidirectional DCR with a sectionalized input source (Smirnov, 2008; Afonina et al. 2004; Smirnov, 2005; Goryachev et al. 1996) is shown in Figure 9.

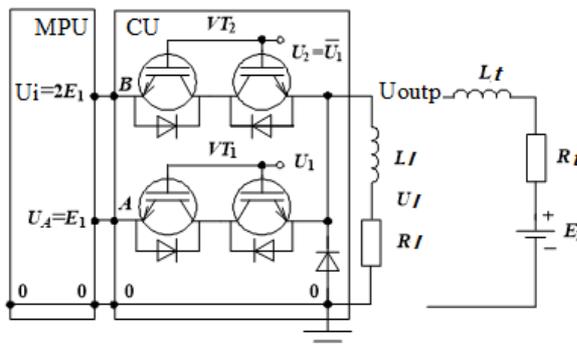


Figure 9. Block-diagram of a bilevel bidirectional DCR with a sectionalized input source in forward and reverse directions

DCR consists of a multi-level power unit (MPU), control unit (CU) and ( $R_H, L_H$ ) load. MPU is intended to form the discrete levels of input voltage spaced apart at regular intervals by the  $E$  value.  $E$  value is equal to the input source voltage  $E_1$  for a step-up DCR, and  $\frac{E_1}{K}$  - for a step-down DCR, and  $K$  - is a number of regulation levels. CU is represented by two PWM regulating elements on the bases of bidirectional transistor keys  $VT_1$  and  $VT_2$ . The main drawback of such DCRs is a big number of regulating transistor keys equal to the number of regulation levels  $K$ .

The use of step-up MDCR on the basis of the switched-capacitor structures allows reducing the number of regulating transistor keys down to two at any number of regulation levels. Efficiency is achieved by managing discrete levels of  $U_A$  and  $U_B$  voltages (Figure 10) by changing the MPU structure (Belenkov, 2002; Vikentyev, 2001; Zubritsky, 2002; Mazur, 2001; Bernardzhevskaya, 2005; Strutynsky et al., 2000; Tailor, 2004).

**6. Bilevel Bidirectional DCR with a Sectionalized Input Source on the Basis of Condenser DC-DC Converters of Resonant Type**

The simplest solution is a bilevel DCR. Block-diagrams of bidirectional bilevel step-up and step-down DCR are identical. The principle of DCR operation in the forward and reverse directions is shown in Figure 9.

The difference lies in the structure of their MPU. Circuit MPU schematics of the step-up and step-down bidirectional bilevel DCRs are shown in Figure 10.

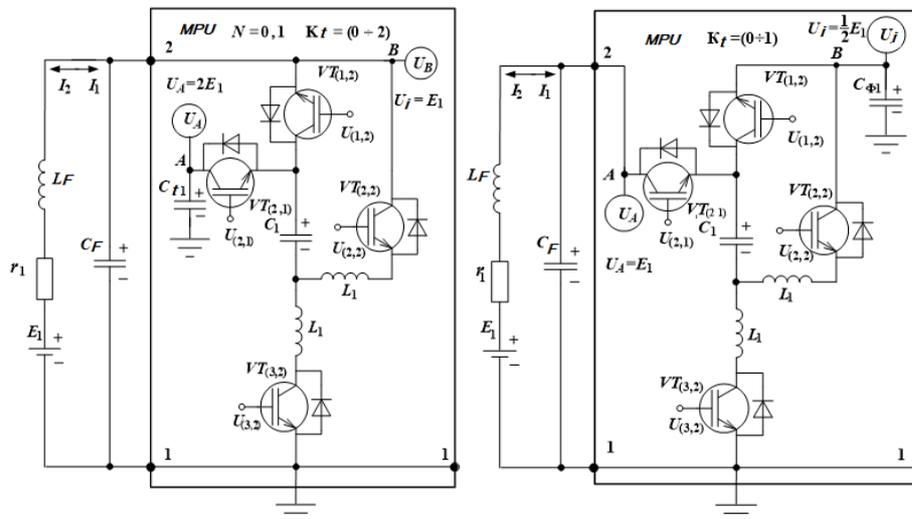


Figure 10. Circuit MPU schematic of the step-up and step-down bidirectional bilevel DCR

These schemes represent a step-up and step-down bidirectional converter modules (BCM), which contain one ( $N = 1$ ) capacitor. Conversion coefficients are equal to  $K_t = (1+N) = 2$  - for an step-up DCR and  $K_t = \frac{1}{1+N} = \frac{1}{2}$  - for a reducing DCR. The principle of MPU power circuit controlling with transistor keys is expedient to be represented by the control matrices. Control matrix consists of a set of control signals  $U_{(i,j)}$  for the corresponding MPU control keys.  $U_{(i,j)} = 0$  - is a control signal, which characterizes the closed state of a transistor key,  $U_{(i,j)} = 1$  - is a control signal, which characterizes the open state of a transistor key,  $U_{(i,j)} = X$  - is a sequence of control pulses with a duration of  $0,5 \cdot T_{\Pi}$ , following with the frequency of  $f_t = \frac{1}{T_t}$ ,  $U_{(i,j)} = \bar{X}$  - is an inverse control signal  $X$ .

Matrices of controlling transistor keys in MPU for step-up (a) and step-down (b) bilevel DCRs (Figure 9.) are given below:

$$U_l = [0, E_1] \quad U_l = [E_1, 2E_1] \quad U_l = \left[0, \frac{1}{2} E_1\right] \quad U_l = \left[\frac{1}{2} E_1, E_1\right]$$

$$\begin{matrix}
 \text{a)} & N=0 & N=0, 1 & \text{б)} & N=1 & N=0, 1 \\
 \begin{vmatrix} U_{(1,1)} & U_{(1,2)} \\ U_{(2,1)} & U_{(2,2)} \\ U_{(3,1)} & U_{(3,2)} \end{vmatrix} & = \begin{vmatrix} - & 0 \\ 0 & 0 \\ - & X \end{vmatrix}, & \begin{vmatrix} - & X \\ 0 & \bar{X} \\ - & X \end{vmatrix}; & \begin{vmatrix} U_{(1,1)} & U_{(1,2)} \\ U_{(2,1)} & U_{(2,2)} \\ U_{(3,1)} & U_{(3,2)} \end{vmatrix} & = \begin{vmatrix} - & X \\ \bar{X} & \bar{X} \\ - & X \end{vmatrix}, & \begin{vmatrix} - & X \\ \bar{X} & 0 \\ - & 0 \end{vmatrix}
 \end{matrix}$$

The main regulating characteristics for step-up (a) and step-down (b) bilevel DCRs in the forward direction are shown in Figure 11.

Operating principle of a bilevel step-up DCR is as follows. In the initial state, the transistor key VT<sub>2</sub> in CU is closed. Voltage of the input source E<sub>i</sub>=U<sub>A</sub> is applied to the input A of the transistor key VT<sub>1</sub>, and voltage 2·E<sub>i</sub>=U<sub>i</sub> is applied to the input B of the transistor key VT<sub>2</sub>. U<sub>i</sub> change occurs in the range [0, E<sub>i</sub>], is carried out at N=0 through the change in duty factor γ<sub>1</sub> of control pulses U<sub>1</sub> of a transistor key VT<sub>1</sub> within the range of [0,1]. Then, to the control input of transistor key VT<sub>2</sub> applied are the control pulses U<sub>2</sub> =  $\bar{U}_1$  and the U<sub>i</sub> adjustment occurs within the range of [E<sub>i</sub>, 2E<sub>i</sub>]. It is carried out at N=0.1 through a simultaneous change in duty factors γ<sub>1</sub> and γ<sub>2</sub>=1 - γ<sub>1</sub>, respectively, within the ranges of [1,0] and [0,1] (Menshikova, 1996; Brodskaya et al., 2009; Han et al., 2011).

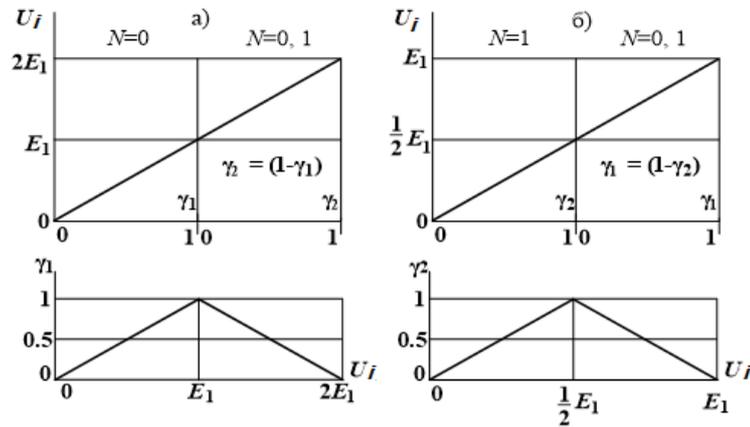


Figure 11. Regulating characteristics of step-up (a) and reducing (b) bilevel DCRs in the forward direction

The work of a bilevel step-down DCR is as follows. In the initial state, the transistor key VT<sub>1</sub> in CU is locked. Voltage  $U_I = \frac{1}{2} \cdot E_1$  from the output of the step-down BCM, which is a part of MPU, is applied to the B input of the transistor key VT<sub>2</sub>. At the same time, voltage of the input source E<sub>i</sub>=U<sub>A</sub> is applied to the A input of the transistor key VT<sub>1</sub>. U<sub>L</sub> adjustment within the range of  $\left[0, \frac{1}{2} \cdot E_1\right]$  is carried out at N=1 through the change in duty factor γ<sub>1</sub> of control pulses U<sub>2</sub> of the transistor key VT<sub>2</sub> within the range of [0,1]. Then, to the control input of transistor key VT<sub>1</sub> applied are the control pulses  $U_1 = \bar{U}_2$  and the U<sub>H</sub> adjustment occurs within the range of  $\left[\frac{1}{2} \cdot E_1, E_1\right]$ . It is carried out at N= 0.1 through a simultaneous change in duty factors γ<sub>2</sub> and γ<sub>2</sub>=1- γ<sub>2</sub>, respectively, within the ranges of [1,0] and [0,1].

Operating principle of the step-up and step-down bilevel DCRs in the reverse direction (regenerative behaviour) is based on the impact of the E<sub>2</sub> source, which is the EMF of load, for example of an electric motor. The matrices of controlling transistor keys in MPU of step-up (a) and step-down (b) bilevel DCRs, at operating in the reverse direction possess the following form:

$$E_2 = [E_1, 2E_1] \qquad E_2 = [\frac{1}{2}E_1, E_1]$$

$$a) \qquad N=1 \qquad b) \qquad N=1$$

$$\begin{vmatrix} U_{(1,1)} & U_{(1,2)} \\ U_{(2,1)} & U_{(2,2)} \\ U_{(3,1)} & U_{(3,2)} \end{vmatrix} = \begin{vmatrix} - & X \\ \bar{X} & 0 \\ - & 0 \end{vmatrix}; \qquad \begin{vmatrix} U_{(1,1)} & U_{(1,2)} \\ U_{(2,1)} & U_{(2,2)} \\ U_{(3,1)} & U_{(3,2)} \end{vmatrix} = \begin{vmatrix} - & 0 \\ 0 & \bar{X} \\ - & X \end{vmatrix};$$

Regulating characteristics at operation of bilevel step-up (a) and step-down (b) DCRs in the reverse direction are demonstrated in Figure 12.

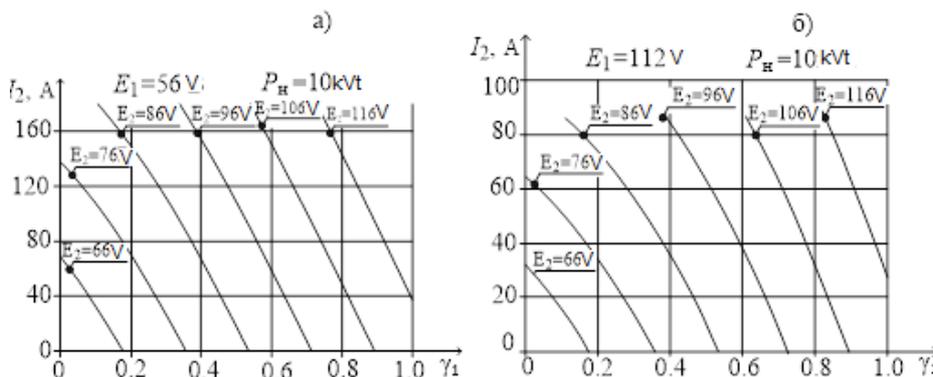


Figure 12. Regulating characteristics at operation of bilevel step-up (a) and step-down (b) DCRs in the reverse direction

They are obtained for the DCR, which load is a DC electric motor. Rated power and voltage of the electric motor are  $P_H=10\text{kW}$ ,  $U_H=110\text{V}$ . At the same time, the armature inductance is  $L=5\text{mH}$ , and value of the primary source voltage for a step-up one is  $E_1=56\text{V}$ , for a step-down one is  $E_1=112\text{V}$ .

Parameters of the elements of step-up and step-down bilevel DCRs are determined by the following expressions:

$$C_1 = \frac{I_{l(\max)}}{f_k \cdot E_1 \cdot \Delta U_{C1}^*}, L_1 = \frac{1}{4 \cdot \pi^2 \cdot f_k^2 \cdot C_1} \text{ for a step-up bilevel DCR,}$$

$$C_2 = \frac{I_{l(\max)}}{2 f_k \cdot E_1 \cdot \Delta U_{C1}^*}, L_1 = \frac{1}{4 \cdot \pi^2 \cdot f_k^2 \cdot C_1} \text{ for a step-down bilevel DCR,}$$

where  $\Delta U_{C1}^* = \frac{\Delta U}{E_1}$  - is a maximum allowed relative ripple of voltage on the capacitor  $C_1$ ,  $I_{H(\max)}$  - is a

maximum current in the load of a bilevel DCR,  $f_k$  - is a switching frequency of the power transistors in MPU. An important property of the considered bilevel regulators is that the levels of voltages applied to all the elements of their power circuit are identical and equal to  $E_1$  - for step-up and  $0.5 \cdot E_1$  - for step-down DCRs. Besides, the currents passing through all the power circuit elements of their MPU are also similar in form and their average values are equal to  $\frac{I_l}{2}$  - for a step-up and  $I_H$  - for a step-down DCR.

**7. Step-Up Three-Level Bidirectional Dcrs with a Sectionalized Input Source on the Basis of Condenser DC-DC Converters of Resonant Type**

An important advantage of step-up DCRs is that the CU consists of two transistor keys (Figure 9) at any number of regulation levels. A power circuit schematic of MPU of a step-up three-level bidirectional DCR is shown in Figure 13. It consists of BCM 1 and BCM 2 possessing the conversion coefficients, respectively  $K_{i1}=(N_1+1)=3$  and  $K_{i2}=(N_2+1)=2$ . A low pass filter ( $L_F, C_F$ ) is intended for ripple smoothing of the current consumed by DCR from the input source  $E_1$ . It may be excluded from the MPU power circuit, if the requirements to the ripple value of the input current are absent. The work of a three-level DCR in the forward direction is as follows. In the initial

state, in BCM 1 and BCM 2 there operate only charging transistor keys  $VT_{(3,2)}$ ,  $VT_{(3,3)}$  and  $VT_{(3,5)}$ . The rest of the MPU keys are locked. Such operating mode maintains the voltage across the capacitors of their PC at the level of  $E_1$ . In CU, closed is the transistor key  $VT_2$ . Input voltage  $E_1 = U_A$  through the bypass diodes of the transistor keys  $VT_{(1,2)}$  and  $VT_{(2,1)}$  from the BCM 1 output is applied to the input A of the transistor key  $VT_1$  in CU. Adjustment of the DCR output voltage  $U_H$  within the range of  $[0, E_1]$  is carried out at  $N_1 = N_2 = 0$  through the change in duty factor  $\gamma_1$  of control pulses  $U_1$  of the transistor key  $VT_1$ . In order to provide the adjustment of  $U_H$  within the range of  $[E_1, 2 \cdot E_1]$  to an input of the discharging transistor key  $VT_{(2,5)}$ , in BCM 2 applied is the control signal  $U_{(2,5)} = \overline{U_{(3,5)}}$ . As a result, the output voltage of BCM 2  $U_1 = (N_2 + 1) \cdot E_1$  is applied to the input of the transistor key  $VT_2$  in CU. The adjustment is carried out at  $N_1 = 0, N_2 = 1$  through a simultaneous change in duty factors  $\gamma_2 = (1 - \gamma_1)$  and  $\gamma_1$  of control pulses  $U_2 = \overline{U_1}$  of the transistor keys  $VT_2, VT_1$ , respectively, within the ranges of  $[0, 1]$  and  $[1, 0]$ .

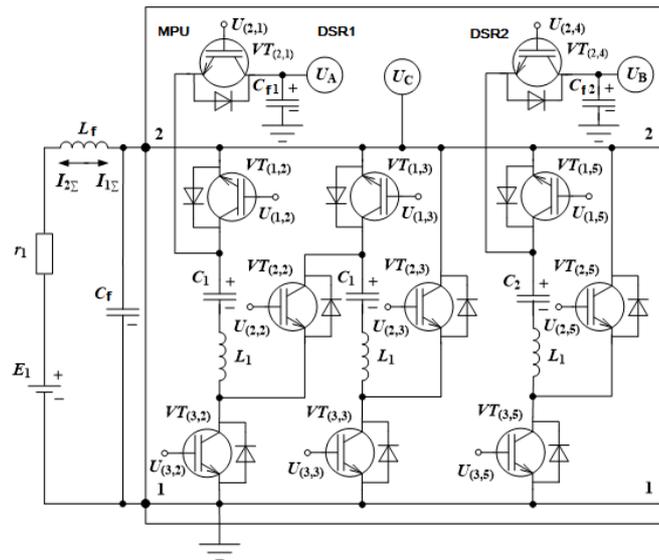


Figure 13. MPU power circuit schematic of a step-up three-level bidirectional DCR

At the final stage,  $U_H$  adjustment occurs within the range of  $[2 \cdot E_1, 3 \cdot E_1]$ . For this purpose, to the control inputs of discharging transistor keys of BCM 1  $VT_{(2,2)}$  and  $VT_{(2,3)}$  applied are the control pulses  $U_{(2,2)} = U_{(2,3)} = \overline{U_{(3,2)}} = \overline{U_{(3,3)}}$ . As a result, all the BCM 1 and BCM 2 capacitors are involved into the conversion process, i.e.  $N_1 = 2, N_2 = 1$  and their output voltages  $U_A = (N_1 + 1) \cdot E_1 = 3 \cdot E_1, U_B = (N_2 + 1) \cdot E_1 = 2 \cdot E_1$  are applied to the inputs of transistor keys  $VT_1$  and  $VT_2$  in CU. At the same time, adjustment is carried out through a simultaneous change in duty factors  $\gamma_1$  and  $\gamma_2$  of control pulses  $U_1 = \overline{U_2}$  of the transistor keys  $VT_1$  and  $VT_2$ , respectively, within the ranges of  $[0, 1]$  and  $[1, 0]$ .

Regulating characteristics of a step-up three-level DCR (Figure 13) at its operation in forward direction is shown in Figure 14a.

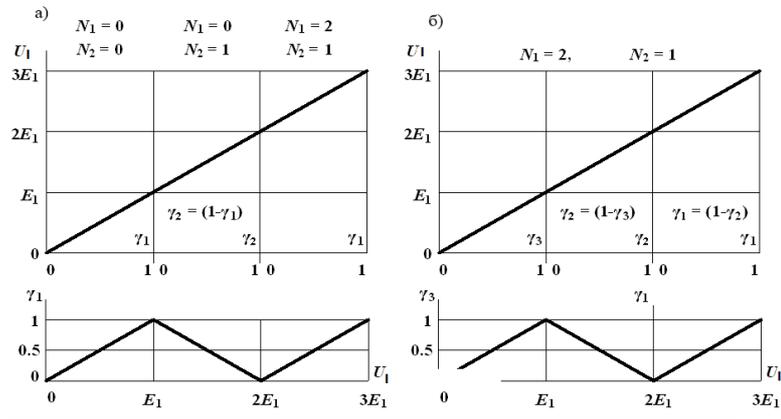


Figure 14. Regulating characteristics of step-up three-level DCRs at their operation in forward direction

Control matrices of the MPU transistor keys at DCR operating in forward direction, for the specified adjustment ranges of UH possess the following form:

$$\begin{matrix}
 U_l = [0, E_1] & U_l = [E_1, 2E_1] & U_l = [2E_1, 3E_1] \\
 N_1=0, N_2=0 & N_1=0, N_2=1 & N_1=2, N_2=1 \\
 \left| \begin{matrix} - & 0 & 0 & - & 0 \\ 0 & 0 & 0 & 0 & 0 \\ - & X1 & X1 & - & X2 \end{matrix} \right|, & \left| \begin{matrix} - & 0 & 0 & - & 0 \\ 0 & 0 & 0 & 0 & \overline{X2} \\ - & X1 & X1 & - & X2 \end{matrix} \right|, & \left| \begin{matrix} - & 0 & 0 & - & 0 \\ 0 & \overline{X1} & \overline{X1} & 0 & \overline{X2} \\ - & X1 & X1 & - & X2 \end{matrix} \right|
 \end{matrix}$$

Matrices of controlling the MPU power circuit keys at regulator’s operating in the reverse direction, for variation ranges  $E_2 = [E_1, 2E_1]$  и  $E_2 = [2E_1, 3E_1]$  possess the following form:

$$\begin{matrix}
 E_2 = [E_1, 2E_1] & E_2 = [2E_1, 3E_1] \\
 N_1=0, N_2=1 & N_1=2, N_2=1 \\
 \left| \begin{matrix} - & 1 & 0 & - & X2 \\ \overline{X1} & 0 & 0 & \overline{X2} & 0 \\ - & 0 & 0 & - & 0 \end{matrix} \right|, & \left| \begin{matrix} - & X1 & X1 & - & X2 \\ \overline{X1} & 0 & 0 & \overline{X2} & 0 \\ - & 0 & 0 & - & 0 \end{matrix} \right|
 \end{matrix}$$

Regulating characteristics of a step-up three-level DCR at its operation in reverse direction are shown in Figure 15.

The main advantage of the DCR under study is the simplicity of its CU. CU consists of only two adjusting transistor keys VT<sub>1</sub> and VT<sub>2</sub>. The effect is achieved by changing the structures of BCM1 and BCM2 in its MPU. The disadvantage is that the change in the number of capacitors in BCM 1 and BCM 2 is accompanied by transient phenomena of voltages at their output capacitors C<sub>F1</sub> and C<sub>F2</sub>. This leads to a delay in setting U<sub>A</sub> and U<sub>B</sub> voltages to the time  $\tau_t \cong 5 \cdot T_k$ . The drawback specified is eliminated, if the structures of BCM1 and BCM2 are not changed during the process of adjustment. However, in this case, it is necessary to introduce the third regulating transistor key VT<sub>3</sub> into CU (Figure 16).

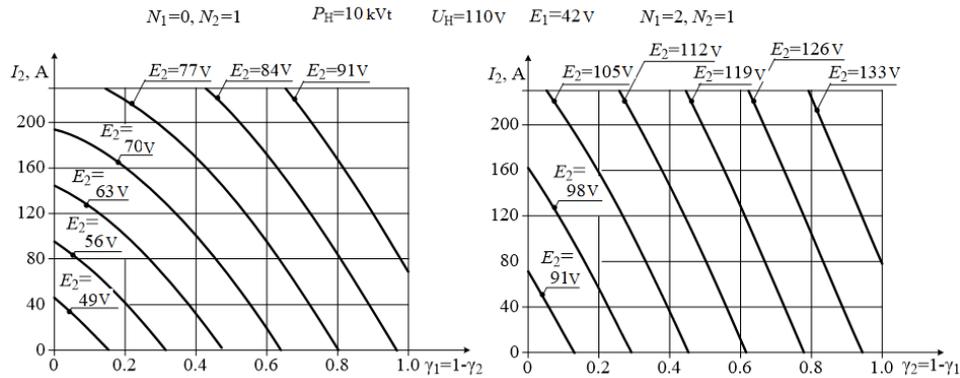


Figure 15. A regulating characteristic of a step-up three-level DCR at its operation in reverse direction

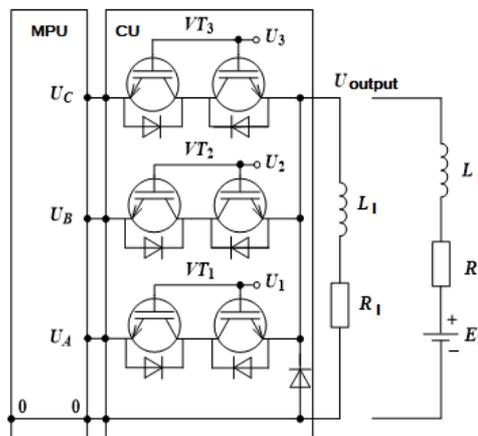


Figure 16. Control unit of the three-level bidirectional DCR with unchangeable structure

In this case, the MPU power circuit (Figure 13) remains unchanged, and the modes of controlling its transistor keys are simplified. The matrices for controlling MPU transistor keys at the DCR operation in the forward (a) and reverse (b) directions in the present case are unchanged in all ranges of regulation and have the following form:

$$\begin{aligned}
 \text{a) } U_1 &= [0, 3E_1] & \text{б) } E_2 &= [E_1, 3E_1] \\
 N_1 &= 2, N_2 = 1 & N_1 &= 2, N_2 = 1
 \end{aligned}$$

$$\left[ \begin{array}{cccc} - & 0 & 0 & - & 0 \\ 0 & X1 & X1 & 0 & X2 \\ - & X1 & X1 & - & X2 \end{array} \right], \quad \left[ \begin{array}{cccc} - & X1 & X1 & - & X2 \\ X1 & 0 & 0 & X2 & 0 \\ - & 0 & 0 & - & 0 \end{array} \right]$$

A regulating characteristic in the forward direction is shown in Figure 14b.

The form of regulation characteristics in the reverse direction is not changed. The difference is that in the left graph (Figure 15) along the axis of abscissas one should delay  $\gamma_3=1-\gamma_2$ .

The weight/volume indicators of DCR are significantly improved through the replacement of BCM 1 and BCM 2 with the bidirectional multicycle resonant converters – BMRC 1 and BMRC 2. BMRC is a  $k$  of parallel connected, identical BCM, working on the total load with a time shift relative to each other by the value

$\Delta t(k) = \frac{T}{k}$  and containing  $N$  capacitors each. The total capacity of the BMRC power circuit

$$C_{\Sigma}(k) = k \cdot N \cdot C_1 = \frac{I_{l \max} \cdot N}{f_t(k) \cdot \Delta U_{c1}} = \frac{I_{l \max} \cdot N}{k \cdot f_t(k=1) \cdot \Delta U_{c1}}$$

is reduced in the inverse proportion to the number of conversion cycles  $k$ , compared to the equivalent in power single-cycle BCM is due to a proportional increase in the frequency of conversion  $f_t(k) = k \cdot f_t(k = 1)$  of its constituent individual BCM.  $f_t(k = 1)$  is a conversion frequency of the equivalent by power, single-cycle BCM. Increase of  $k$  also leads to a significant reduction in capacity  $C_{F1}$ . It is reduced by  $2 \cdot K^2$  times – for odd and by  $K^2$  times – for even  $K$  values. In order to minimize the harmonic distortion factor of the input current  $I_{1\Sigma}(t)$ , consumed by the regulator from the primary source  $E_1$  in the forward direction, and delivered to the source  $E_1$  at regeneration, the signals for controlling respective transistor keys in BMRC1 and BMRC2 – X1 and X2 are shifted with respect to each other. The time shift  $\tau_k$  is chosen from the condition for square minimum of the effective value of total input current  $I_{1\Sigma}(t)$  - in the forward direction, and of total output current  $I_{2\Sigma}(t)$  - in the reverse direction

$$I_{1\Sigma}^2 = \frac{1}{T_t} \cdot \int I_{1\Sigma}^2(t) \cdot dt = \frac{1}{T_t} \int [I_{1MPU1}(t) + I_{1MPU2}(t - \tau_k)]^2 \cdot dt - \min,$$

Since the permanent components of the currents  $I_{1MRC1}(t)$ ,  $I_{1MRC2}(t)$  in both directions, do not depend on the time shift  $\tau_k$  then is clear that the defined criteria shall also mean the minimization of square of the effective value  $I_{1\Sigma}^2(\sim)$  of the variable component of input current  $I_{1\Sigma}(t) = I_{1MRC1}(t) + I_{1MRC2}(t)$ .

Solution of the problem set for the values  $k_1 = k_2 = k \geq 1$  provides the following expression for the optimal

time shifts  $\tau = \frac{T_t}{k \cdot 2 \cdot k}$  and  $\tau = \frac{T_t}{k \cdot 4 \cdot k}$ , respectively, for even and odd values of  $K$ . Parameters of the elements of

the step-up and step-down, bilevel DCRs are determined by the following expressions:

$$C_1 = \frac{I_{l(\max)}}{f_k \cdot E_1 \cdot \Delta U_{C1}^*}, L_1 = \frac{1}{4 \cdot \pi^2 \cdot f_k^2 \cdot C_1} \text{ for a step-up bilevel DCR,}$$

$$C_2 = \frac{I_{l(\max)}}{2 f_k \cdot E_1 \cdot \Delta U_{C1}^*}, L_1 = \frac{1}{4 \cdot \pi^2 \cdot f_k^2 \cdot C_1} \text{ for a step-down bilevel DCR,}$$

### 8. Step-Up Three-Level Bidirectional DCRs with a Midpoint and a Sectionalized Input Source on the Basis of Condenser DC-DC Converters of Resonant Type

Multilevel DCRs with the midpoint possess the easiest MPU (Figure 17). Simplification is achieved by using intermediate points in the MPU circuit for obtaining voltages of discrete levels  $E_1, 2 \cdot E_1, 3 \cdot E_1$ , required for the operation of a step-up MDCR.

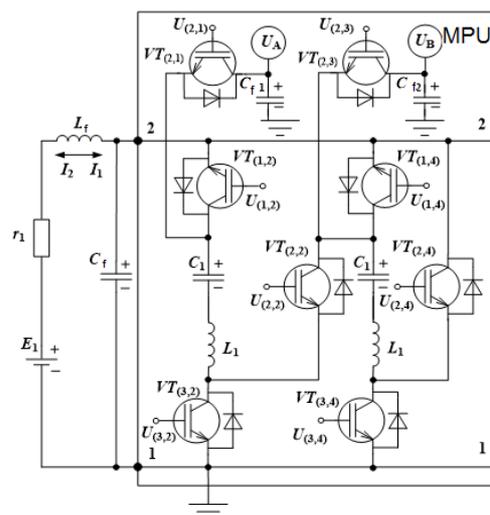


Figure 17. MPU circuit schematic of a step-up three-level DCR with a midpoint

In a step-up three-level DCR with a midpoint, for obtaining voltage  $2 \cdot E_1$  used is the connection point of the collector of the intermediate discharging transistor key  $VT_{(2,2)}$  with a positive plate of the capacitor  $C_1$  in BCM 1. In this case, BCM 2 is excluded from the MPU power circuit. As a result, the power circuit of a step-up three-level MPU is simplified by three IGBT transistor keys and one capacitor. The main drawback of such DCR is related to the asymmetry of its power circuit operation. It is conditioned by the difference in discharge currents of capacitors  $C_1$  of different chains. This makes it difficult to provide a soft-switching mode of transistor keys included into the MPU. By increasing capacitance of the capacitors  $C_1$  and  $C_{\phi 1}$ ,  $C_{\phi 2}$  this drawback disappears. However, such method of its eliminating degrades the weight/volume indicators of MDCR as a whole. The weight/volume indicators of DCR with a midpoint are significantly improved through replacement of its BCM by a bidirectional multicyle resonant converter (BMRC) with a midpoint. Figure 18.

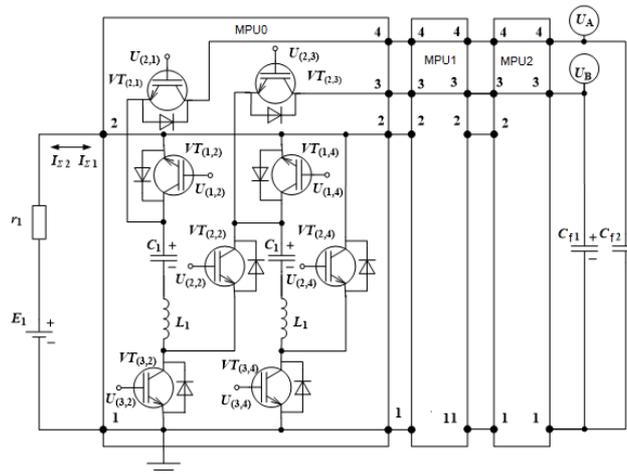


Figure 18. BMRC with a midpoint circuit schematic

Type of adjusting characteristics of the DCR with a midpoint in forward and reverse directions totally coincides with the characteristics given in Figure 14 and Figure 15 for a three-level DCR, Figure 13 (Rydell-Tormanen et al., 2012).

## 9. Summary and Conclusions

Analysis of the characteristics of the SEI (PAM) and SEI (PWM) specified allows the following conclusions.

1. When the initial value of the process of filling coefficients  $\gamma(3,2) = \gamma(3,3) = \gamma(2,1) = 0,5$  of SEI (PAM) and SEI (PWM) operate in a continuous transmission of electric energy, that is, the system controls the charging and PD bit keys. In this case, the system works as an ideal transformer currents and efficiencies of PAM and PWM ESR identical and are defined by expressions (2) and (3).
2. From the analysis of the adjustment characteristics (Figure 7.8) shows that with the increase in the value of the inductance  $L_1$  regulated power ESR (PWM) decreases, its Efficiency according to equations (1) and (2) increases.
3. Subject to the boundary conditions, tolerances  $E1_{max}$ ,  $E2_{max}$  and setpoint power sources  $E_1$  and  $E_2$ , made adjustments to the settings, and the Efficiency remains unchanged as shown by the expressions (4) and (5).
4. The regulation characteristics analyzing (Figure 7.8) shows that the middle of the linear portion (operating point) dependences  $P_2 [\gamma(3, i)]$ ,  $P_1 [\gamma(2,1)]$  for all considered variables  $L_1$  corresponds to the value of the loop parameter  $\gamma(3, i) = \gamma(2,1) = 0,275$ .
5. Considered are the principles of construction and operation of bidirectional multi-level DCRs with a sectionalized input source on the basis of condenser DC-DC converters of the resonant type.
6. Introduced is the concept of control matrix, giving an idea of the algorithm for controlling transistor keys of the DCR power circuit and allowing to simplify the development of a circuit and its management.
7. Obtained are the adjusting characteristics of DCR at its operation in the forward and reverse directions.
8. Obtained are the formulas for calculating parameters of the DCR power circuit elements.
9. It is demonstrated that the application of multicyle DCRs allows not only reducing the current's harmonics

factor of the consumed primary source, but also significantly reducing the amount of the total capacitance of its power circuit.

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