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Analysis of Active Clamp Fly Back Converter

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Abstract

This paper proposes an active-clamp fly back dc-dc converter using an isolated transformer. This converter consists of two switches namely auxiliary and main switch. The auxiliary switch is mainly added to reduce the voltage ripples especially on the primary side of the isolated high frequency transformer. This in turn will reduce the voltage stress present at the main switch. Active clamping is done for the recycling of stored energy in the HT and also to ensure the ZVS operation. The voltage spikes during transistor turn off time are clamped by active clamping. The Zero Voltage Switching (ZVS) of the main switch is obtained mainly using the auxiliary switch and the clamp capacitor. Analysis of active clamped fly back converter is done for 120W. The analysis is done for various switching frequencies and delay values for proper core reset.

Keywords: isolated dc-dc converter, high frequency transformer (HT), Zero Voltage Switching (ZVS), active clamping

1. Introduction

The flyback converter has its wide applications such as switched mode power supplies [1], where step down of voltage in a laptop down to the few volts needed by the processor is required, LED lighting systems with PV source [2] and LCD backlights. In LED lighting systems, any buck boost converter can be used for charging the battery and the proposed fly back converter can be used as a discharger to drive the LEDs in traffic signals as shown in Figure.1.At present forward converter has been used as a discharger. Instead of forward converter, Fly back converter can also be used because in both these applications, low power and low voltage is required at the output, this requirement is fulfilled by this proposed converter without the risk of extreme duty ratios. This advantage is notable as high duty ratio increases the secondary side current, losses and hence the size of the output capacitor [3]. As this converter fully utilises the transformer leakage energy, no additional snubber circuit is required. Though the passive clamped circuit also fully utilises this stored energy, the efficiency is not much when compared with the active clamped circuit. The current flowing through the magnetising inductor is made negative by the active clamp circuit to avoid the discontinuous conduction mode operation (DCM) [3]. This topology is selected for its less complex ZVS operation and high efficiency.The primary objective of this paper is to analyse the operation of a Fly back converter and to improve its performance by introducing certain delay time and also by resetting the core effectively.

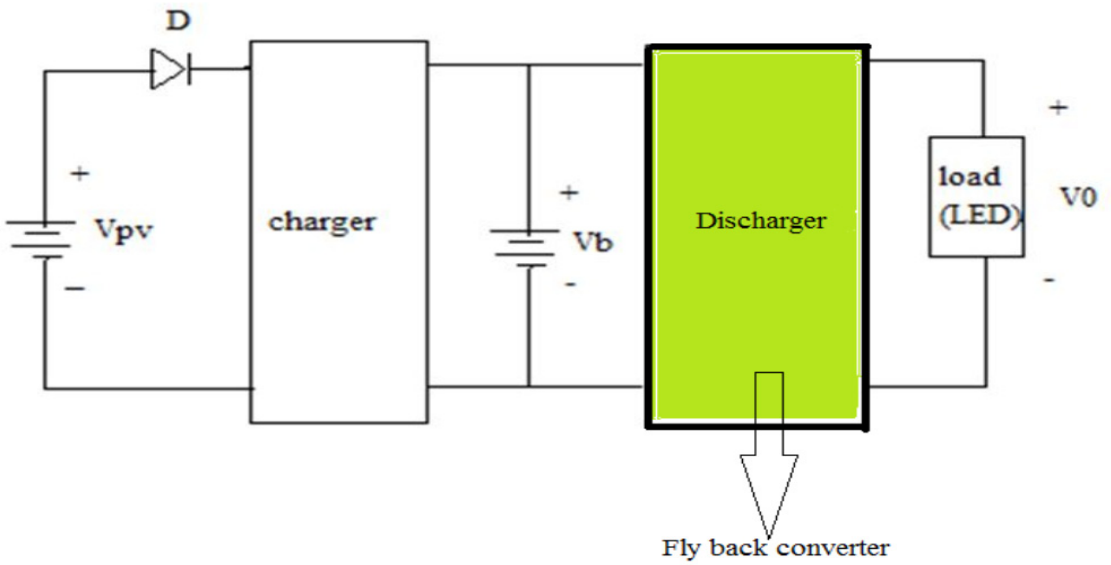

Figure 1. Active clamp fly back converter in LED lighting

2. Proposed System

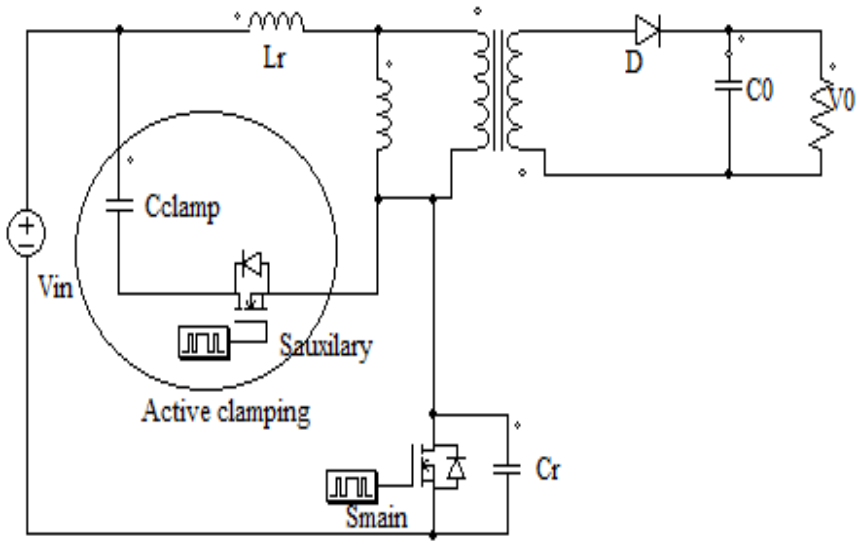

Figure 2. Circuit configuration of active clamp fly back converter

The circuit configuration of active clamp fly back converter is shown in Fig: 2.This circuit consists of two mosfet switches (Saux and Smain), clamp capacitor (Cclamp), diode (D0), transformer, resonant capacitor (Cr) and inductor (Lr).The clamp capacitor and the auxiliary mosfet switch together constitutes the active clamping circuit. The clamp capacitance value will affect the secondary current waveform through the transformer. The load may be selected depending upon the applications. The values of resonant components (Lr and Cr) are appropriately chosen so as to bring the ZVS operation. This resonant component of inductance (Lr) must be selected so that it should not exceed the value of magnetizing inductance (Lm) (i.e.,) Lm must always be greater than Lr. Lr helps in achieving soft switching characteristics [4]. In addition to this, a small dead time (delay time) is added during the turn on of main switch (Smain) to account for ZVS operation. Analysis is done for various values of delay time. The transformer primary to secondary turns ratio is selected as 8:1.

3. Operating Principle of the Proposed Converter

From Fig: 3(a), it is clear that a single cycle consists of eight modes whose time interval varies from t0-t8.

Mode 1: (t0-t1):

During this interval, the switches Smain is turned on while the auxiliary switch Saux is in off condition, so the current flows through the resonant inductor (Lr), magnetizing inductance (Lm) and the main switch (Smain). The secondary side of the transformer remains unconducting as D0 is in off state. The voltage across the clamp capacitor is nV0 and the current does not flow through this clamp capacitor in this mode. As current flows through the main switch, the voltage across the capacitor Cr is found to be zero. The voltage through the primary side of the transformer may be expressed as

$$Vpri = Vin \times \frac{Lm}{Lm+Lr} \tag{1}$$

And its corresponding primary side current may be expressed as

$$iLm(t) = iLr\ (t) = iLm(t0) + \frac{Vin}{Lm+Lr}(t - t0) \tag{2}$$

The same current at the end of this interval can be found by replacing t=t1.

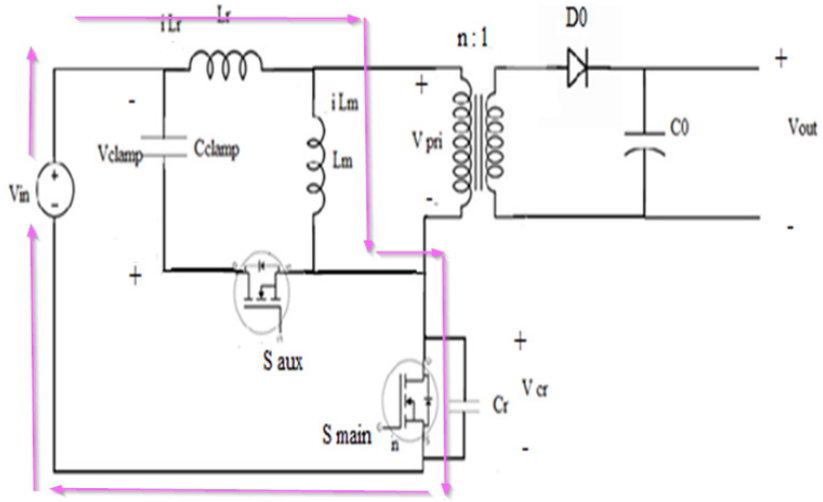

Figure 3(a). Mode 1: (t0-t1)

Mode 2: (t1-t2):

This mode starts when t becomes t1 during which the main switch Smain is turned off. So the current takes the path of resonant circuit which involves Lr, Lm and Cr. Cr is charged by the current flowing through the Lr and Lm.The voltage and current through the resonant capacitors can be given by

$$Vcr(t) = Vin(1 - \cos(w1(t - t1))) + iLr(t1)z1\sin\ (w1(t - t1)) \tag{3}$$

$$iLr(t) = iLr(t1)\cos(w1(t - t1)) + \frac{Vin}{z1}\ \sin\ (w1(t - t1)) \tag{4}$$

Where $w1 = \frac{1}{\sqrt{Cr(Lm+Lr)}}$, $z1 = \sqrt{\frac{Lm+Lr}{Cr}}$

The clamp capacitor still maintains the voltage of nV0.This mode ends when t becomes t2.The primary side voltage of the transformer can be given by

$$Vpri(t) = Vin - Vcr(t) = Vin - \frac{iLr(t1)}{Cr}(t - t1) \tag{5}$$

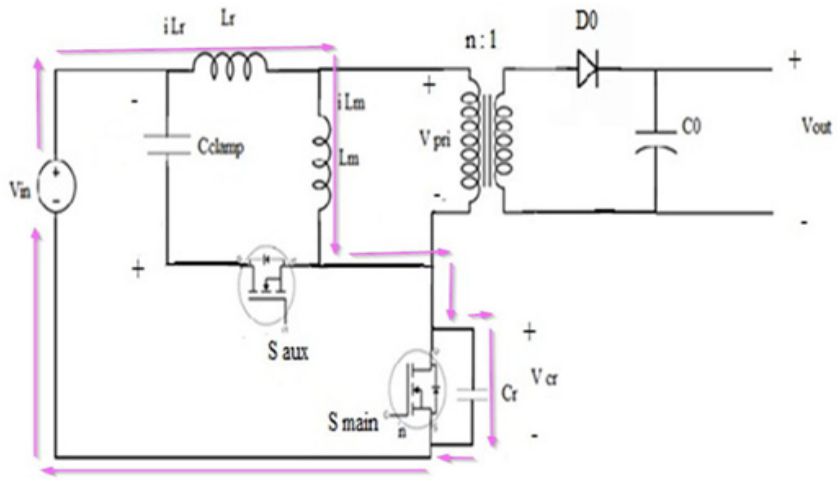

Figure 3(b). Mode 2: (t1-t2)

Mode 3: (t2-t3):

The beginning of this mode is indicated by the turning on of the body diode in the auxiliary switch (S aux). The energy stored during the modes 1 and 2 is now used to charge the clamp capacitor. The entire value of current flowing through Lm charges the Cclamp due to its large value when compared to Cr. And this clamp and resonant capacitor voltage and current can be given as

$$Vclamp(t) = nV0\cos\big(w2(t-t2)\big) + iLr(t2)z2\sin\big(w2(t-t2)\big) \quad (6)$$

$$i\ clamp(t) = iLr(t) = iLr(t2)\cos\big(w2(t-t2)\big) - \frac{nV0}{z2}\sin\left(w2(t-t2)\right) \quad (7)$$

$$Vcr(t) = Vin + nV0\cos\big(w2(t-t2)\big) + iLr(t2)z2\sin\left(w2(t-t2)\right) \quad (8)$$

Where $w2 = \frac{1}{\sqrt{Cclamp(Lm+Lr)}}$, $z2 = \frac{(Lm+Lr)}{Cclamp}$

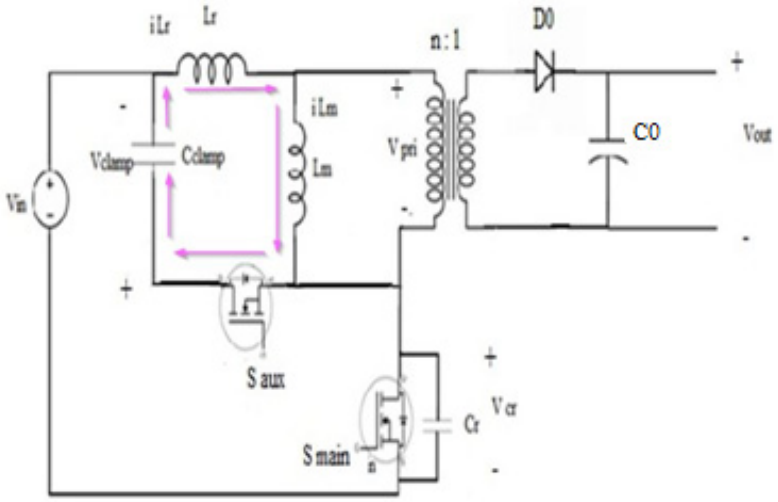

Figure 3(c). Mode 3: (t2 –t3)

Mode 4: (t3-t4):

When t=t3, the primary side voltage is decreased to –nV0 and Saux must turn on before the current through the clamp capacitor reverses its polarity to ensure ZVS operation. Now the diode D0 is forward biased by the secondary transformer voltage. So the spike voltages during turn off time of Smain are clamped by the output capacitor. The current through the magnetising inductance can be expressed as,

$$iLm(t) = iLm(t3) - \frac{nV0}{Lm}(t - t3)$$

Now the current next passes through the clamp capacitor and its corresponding voltage and current can be expressed as,

$$Vclamp(t) = nV0 - \big(nV0 - Vclamp(t3)\big)\cos\big(w3(t - t3)\big) + iLr(t3)z3\sin\,(w3(t - t3)) \quad (10)$$

$$iclamp\,(t) \approx iLr = \frac{(nV0 - Vclamp(t3))}{z3}\sin\,(w3(t - t3) + iLr(t3)\cos\big(w3(t - t3)\big)) \quad (11)$$

The secondary side diode current can be given as,

$$iD0(t) = n(iLm(t) - iLr(t)) \quad (12)$$

Where

$$w3 = \frac{1}{\sqrt{CclampLr}}, \qquad z3 = \sqrt{\frac{Lr}{Cclamp}}$$

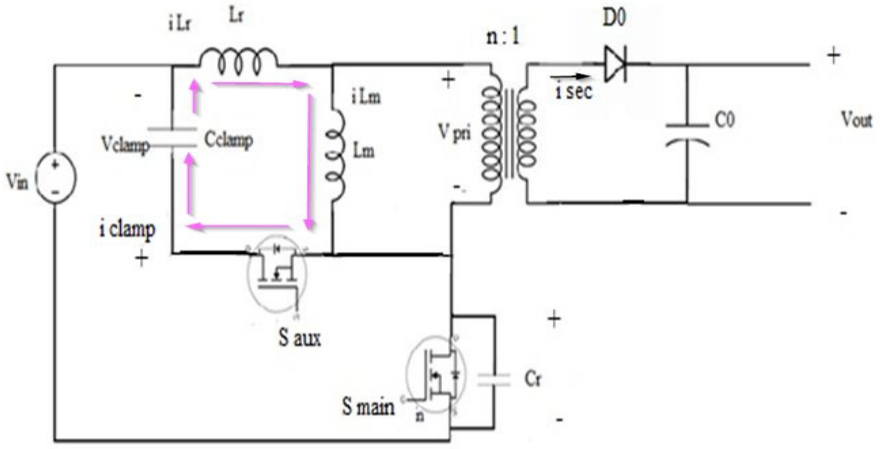

Figure 3(d). Mode 4: (t3-t4)

Mode 5: (t4-t5):

At t=t4, the auxiliary switch Saux is turned off. The current takes the path of Lr and switch parasitic capacitances. The current through the clamp capacitor again reverses its polarity in this mode, except this all the remaining analysis remains the same.

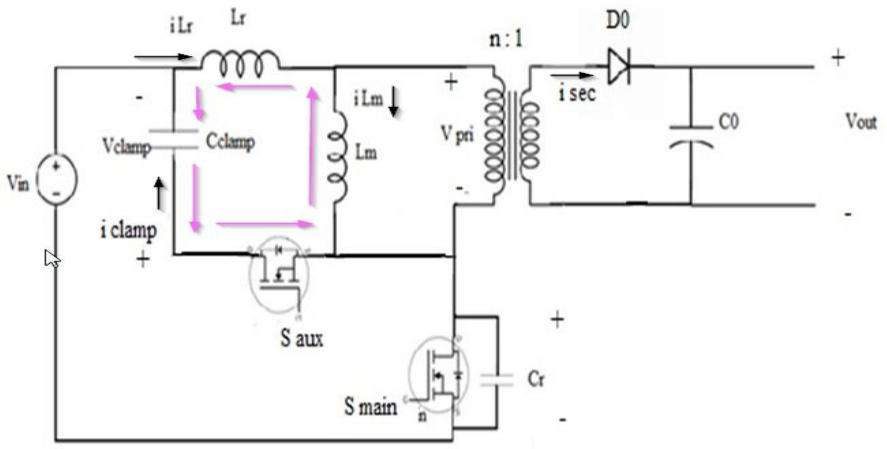

Figure 3(e). Mode 5: (t4-t5)

Mode 6: (t5-t6):

The beginning of this mode is indicated by the turning off of the auxiliary switch so the current through Lm takes the path of the resonant circuit which includes Lr and Cr. The current through Lm can be given as,

$$iLm(t) = iLm(t5) - \frac{nV0}{Lm}(t - t5) \tag{13}$$

The diode D0 still remains in the on time and the primary side voltage is maintained as –nV0.The resonant circuit voltage and current is found to be,

$$Vcr(t) = Vin + nV0 - \big(Vin + nV0 - Vcr(t5)\big)\cos\,(w4(t - t5) + iLr(t5)z4\sin\,(w4(t - t5)) \tag{14}$$

$$iLr(t) = iLr(t5)\cos\big(w3(t - t5)\big) + \frac{(Vin+nV0-Vcr(t5))}{z4}(\cos\,(w4(t - t5)) \tag{15}$$

Where $w4 = \frac{1}{\sqrt{CrLr}}$ and $z4 = \sqrt{\frac{Lr}{Cr}}$

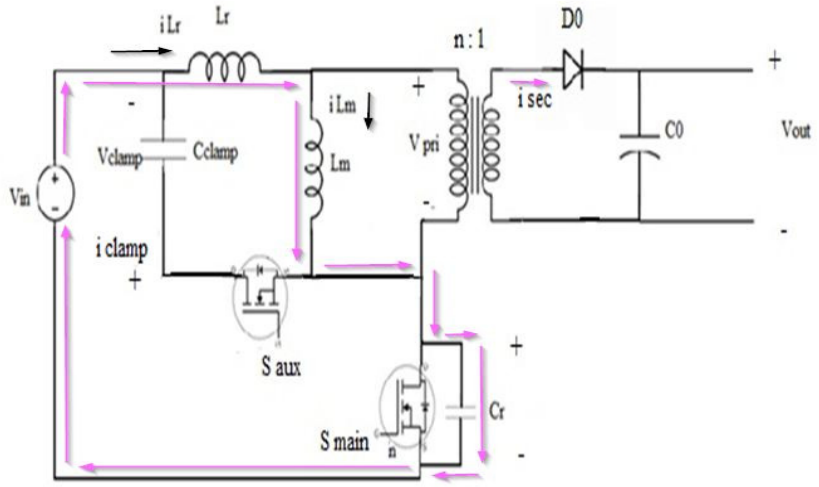

Figure 3(f). Mode 6: (t5-t6)

The current through the clamp capacitor is zero and its voltage is maintained at nV0 and the diode current remains the same as in mode 5.

Mode 7: (t6-t7):

Initially at t=t6, the body diode of Smain is turned on and the resonant capacitor voltage Vcr becomes zero. The current of the resonant leakage inductor can be given by

$$iLr(t) = iLr(t6) + \frac{(Vin+nV0)}{Lr}(t - t6) \tag{16}$$

and the current through the magnetising inductor is given by

$$iLm(t) = iLm(t6) - \frac{nV0}{Lm}(t - t6) \tag{17}$$

The secondary side current of the transformer is characterised by the negative current slope in this mode and it can be given by

$$\frac{diD0}{dt} = -n\left(\frac{nV0}{Lm} + \frac{Vin+nV0}{Lr}\right) \approx -n\frac{Vin+nV0}{Lr} \tag{18}$$

And the secondary side diode current remains the same as equation (12).The main switch must be turned on before iLr becomes positive which is to make sure of ZVS operation.

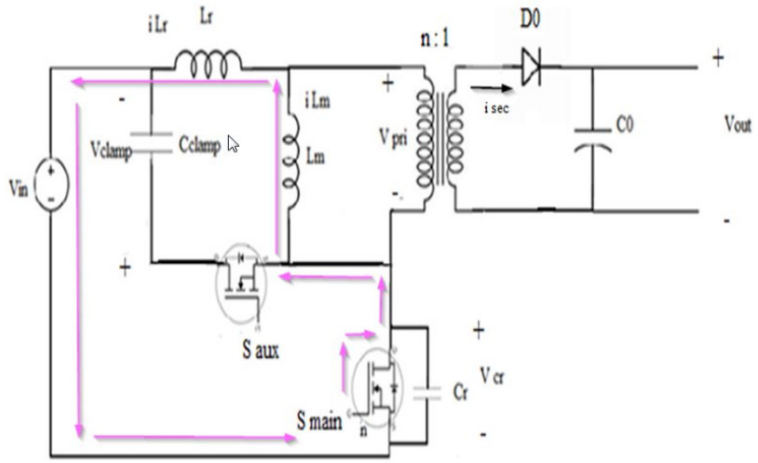

Figure 3(g). Mode 7: (t6-t7)

Mode 8: (t7-t8):

In this mode, main switch is in on state and so the current flowing through resonant inductor iLr begins to increase and the diode current starts decreasing and it reaches zero at t=t0.The voltage and current expressions at the end of single pulse can be given by,

$$Vpri(t) = -nV0$$

$$Vcr(t) = 0 \ , \ Vclamp(t) = nV0 \ \text{ and } \ i\,clamp(t) = 0$$

$$iLr(t) = iLr(t7) + \frac{(Vin+nV0)}{Lr}(t - t7) \tag{19}$$

$$iLm(t) = iLm(t7) - \frac{nV0}{Lm}(t - t7)$$

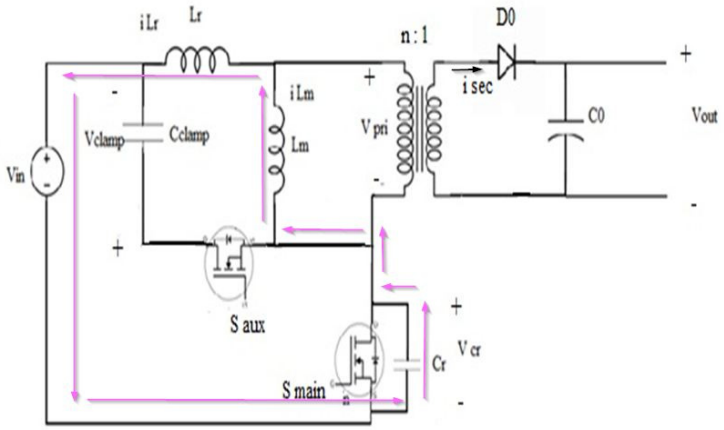

Figure 3(h). Mode 8: (t7-t8)

4. Design Parameters

The proposed converter is designed with a maximum duty cycle of Dmax.The resonant inductor value is taken as 17μH and the resonant capacitor value is found to be 1.5nF.The various parameters are calculated as follows:

PARAMETERS	DESIGN EQUATIONS
Turns ratio	$n = \frac{N1}{N2} = \frac{Vin\ min}{V0}\ \frac{Dmax}{1 - Dmax}$
Clamp capacitance	$Cclamp = \frac{[(1 - Dmin\ Vin)Tsw]^2}{\pi^2 Lr}$
Resonant inductance	$Lr > \frac{Cr(Vin\ \max + nV0)^2}{Is\ main, p^2}$
Output capacitance	$C0 = \frac{Dmax.P0}{fsw.V0.\Delta V0}$

where

$$Ismain, p = \frac{P0}{\eta.Vin\ min.Dmax} + \frac{Vin\ min}{Lm} Dmax.Tsw \tag{20}$$

is the maximum current of the main switch and its voltage stress can be given by

$$Vs\ main\ max = Vin\ \max + nV0 + iLr(t3)z3 \tag{21}$$

Similarly the voltage stress and peak current of the diode can be given as

$$VD0\ max = \frac{Vin\ max}{n} + V0 \tag{22}$$

$$ID0, p = \frac{2P0}{V0(1-Dmax)} \tag{23}$$

5. Analysis of Proposed Converter

Fig 4a. shows the gating pulse of the auxiliary and main switches of the active clamped fly back converter.

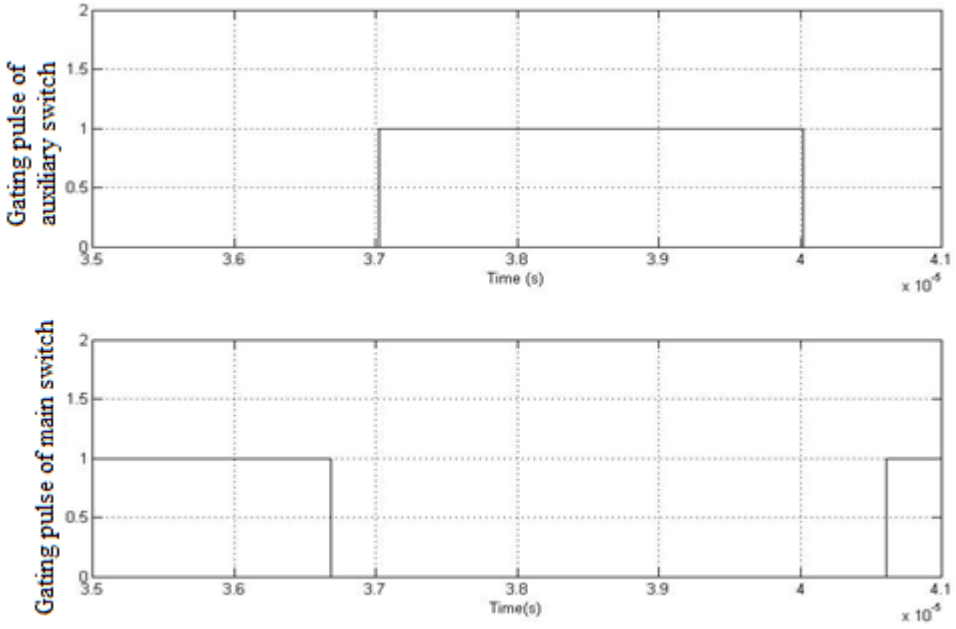

Figure 4(a). Gating pulse for main and auxiliary switch

The current and voltage across the clamp capacitor is shown in Figure 4b. It is evident that Vclamp reaches maximum when iclamp reaches zero.

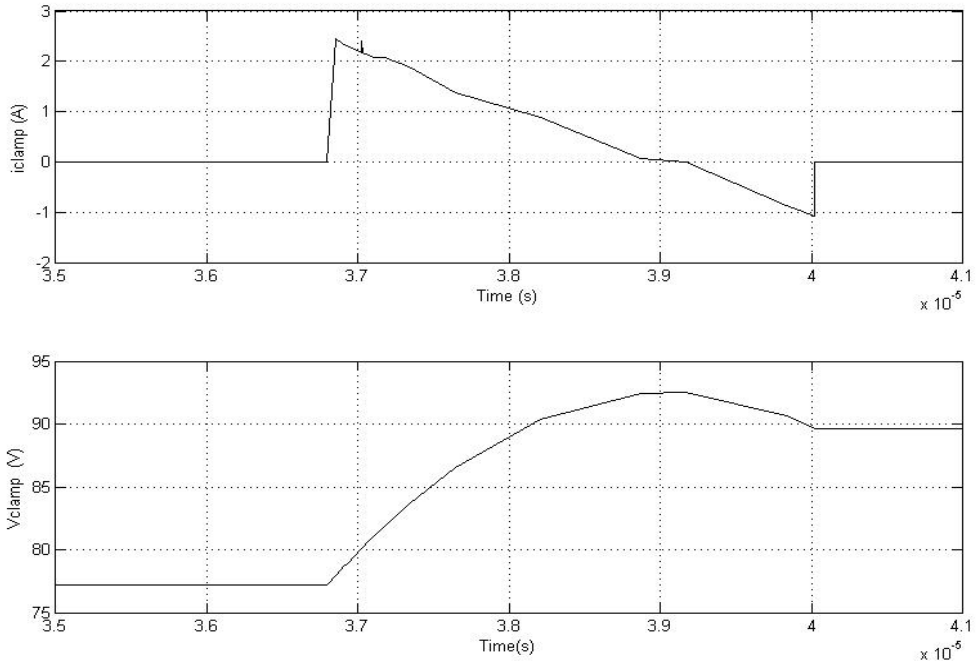

Figure 4(b). Current and voltage waveforms of the clamp capacitor

The maximum value of voltage through the clamp capacitor is 92 v in this time interval. The current through the magnetising and resonant inductor is shown in Figure4c.

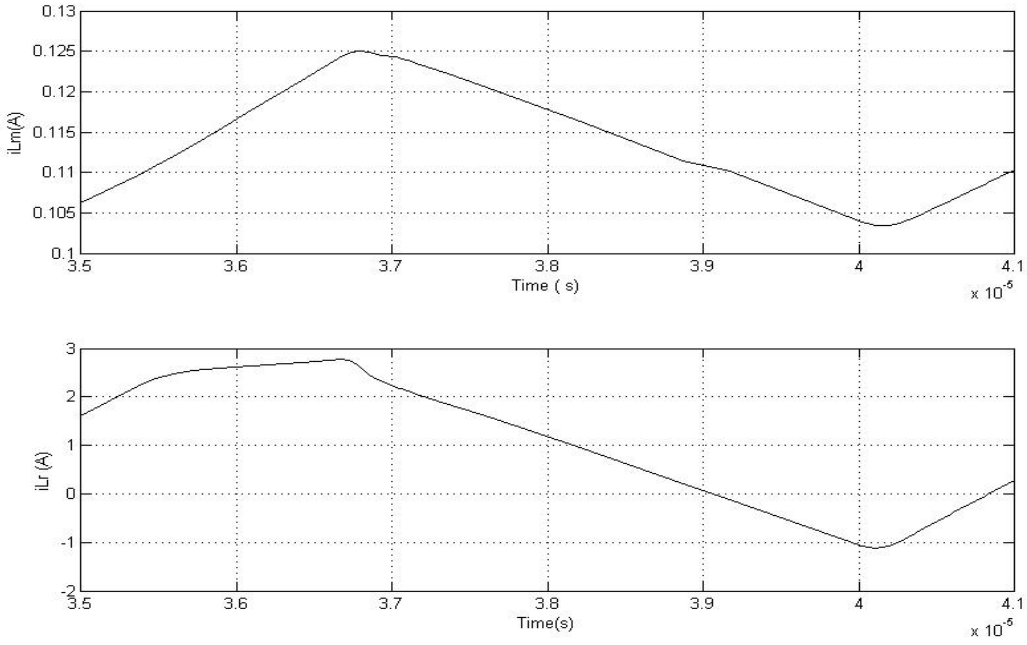

Figure 4(c). Current through the Lm and Lr

The voltage in the primary side of the transformer and the voltage through the resonant capacitor Cr is shown in Figure 4d.

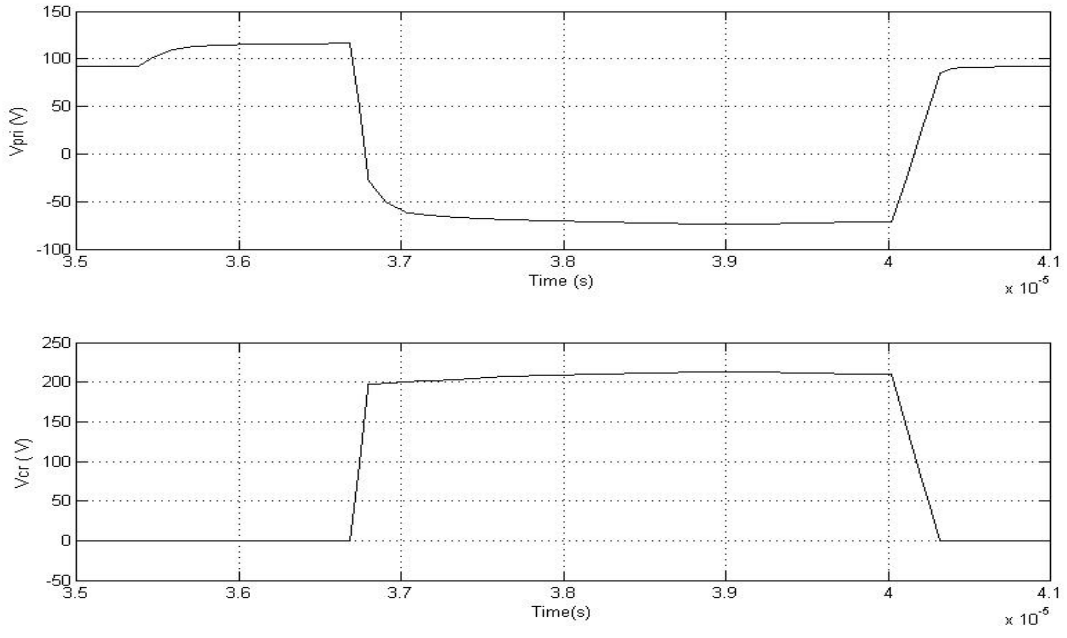

Figure 4(d). Primary voltage and voltage across Cr

The proposed converter is simulated and the results are analysed as follows. The switching frequency of the mosfet is varied and the analysis is shown in Figure 5.

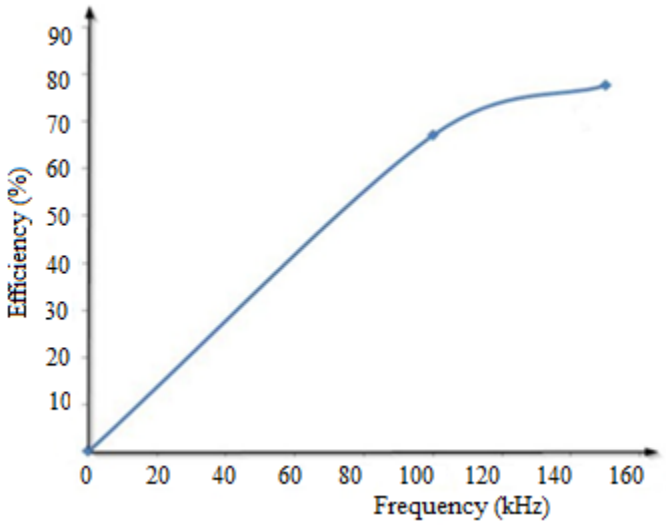

Figure 5. Frequency Vs Efficiency

From Figure 4, it is found that the optimum value of switching frequency is 150 kHz. The ZVS operation of the main switch can be ensured by introducing a delay time in the gating pulse.Now keeping optimum switching frequency, further analysis is done for various delay times. Figure 6 shows the variation of efficiency with delay time with fsw=150 kHz.

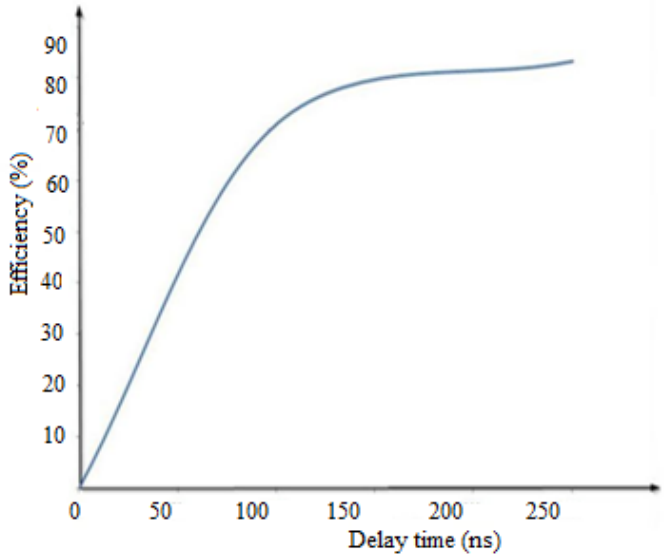

Figure 6. Variation of efficiency with delay time

The comparison of output voltage across the load with delay and without delay for 120 V input supply and 150 kHz switching frequency is shown in Figure 6.The delay period introduced is 250ns.By introducing the delay time, it is found that the voltage stress across the main switch and diode is reduced considerably, which is a notable advantage. The comparison of output voltage with and without delay is shown in Figure 7.

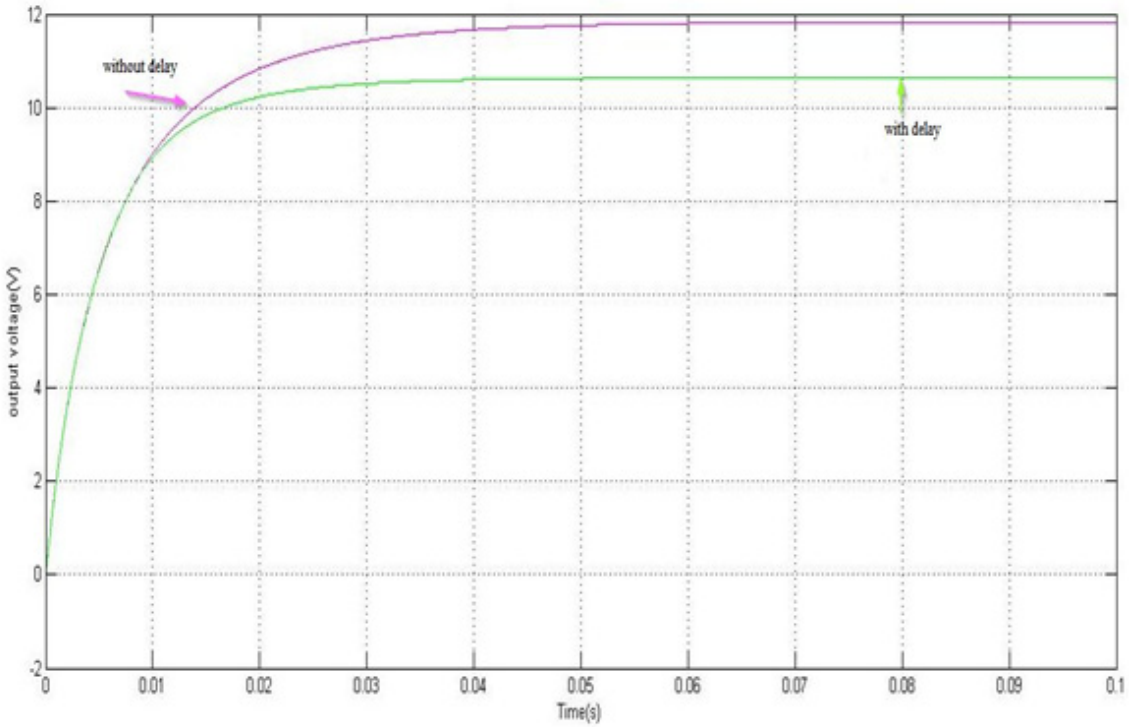

Figure 7. Output voltage with and without delay

The voltage stress across the main switch and diode with delay as 100ns is shown in Figure 8.

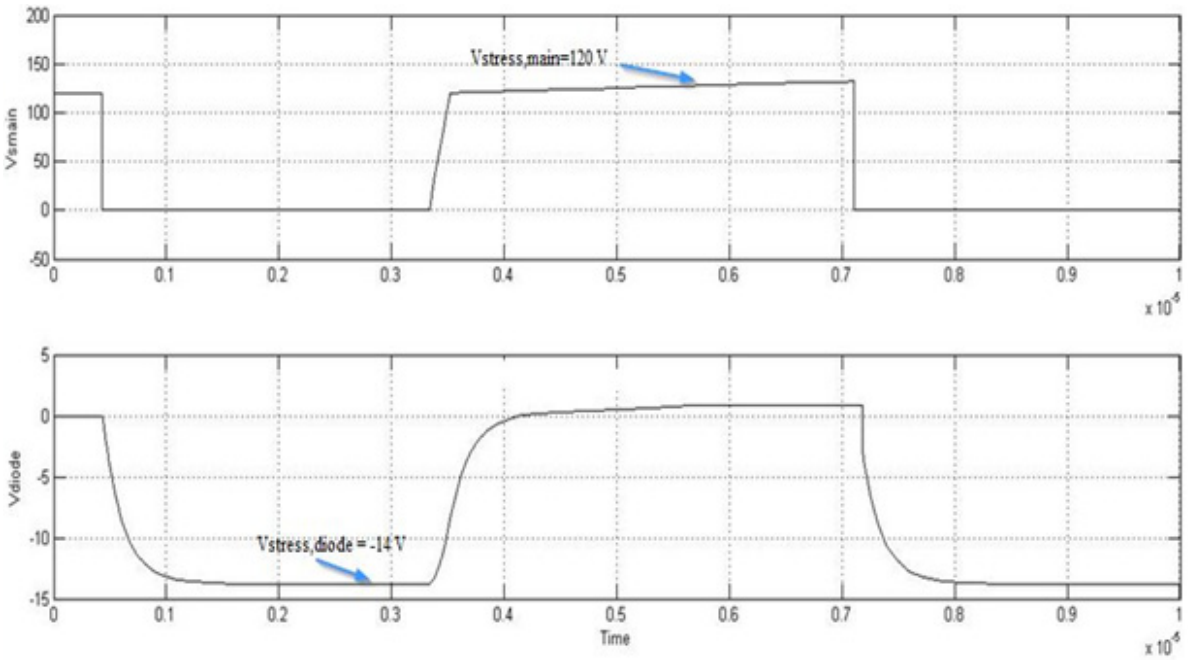

Figure 8. Voltage stress across Smain and diode

Table 1. Voltage stress with and without delay

	WITHOUT DELAY	WITH DELAY=250ns
Vs main	116 V	111 V
Vdiode	12.4 V	11.8 V

From Figure 4, 5 and 6, it can be observed that the optimum value of switching frequency is 150 kHz and the suitable delay time is 250 ns. And from table: 1, it can be seen that introducing a delay reduces the voltage stress across the switches and diode.

6. Conclusion

The mathematical analysis of the proposed converter along with its operation is analysed in this paper. This active clamp fly back converter has the following advantages:

1) This active clamp fly back converter can be used in places where low voltage is required.
2) This proposed converter satisfies the requirement of low voltage and low power without the risk of extreme duty ratios.
3) The voltage stresses across the main switch and the rectifier diode is considerably reduced.
4) The introduction of delay time to active clamping have reduced the switching losses and increased the performance considerably.
5) ZVS operation can be ensured by the introduction of proper delay time.

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