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Low Power Operational Amplifier in 0.13um Technology

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Abstract

Low power is one of the most indispensable criteria in several of application. In this paper a low power operational amplifier consists of two stages and operates at 1.8V power. It is designed to meet a set of provided specification such as high gain and low power consumption. Designers are able to work at low input bias current and also at low voltage due to the unique behavior of the MOS transistors in sub-threshold region. This two-stage op-amp is designed using the Silterra 130nm technology library. The layout has been draw and its area had been calculated. The proposed two stage op-amp consists of NMOS current mirror as bias circuit, differential amplifier as the first stage and common source amplifier as the second stage. The first stage of an op-amp contributed high gain while the second stage contributes a moderate gain. The results show that the circuit is able to work at 1.8V power supply voltage (VDD) and provides gain of 69.73dB and 28.406MHz of gain bandwidth product for a load of 2pF capacitor. Therefore, the power dissipation and the consistency of this operational amplifier are better than previously reported operational amplifier.

Keywords: op-amp, two-stage, miller capacitor, gain, ICMR, PSRR, CMRR, slew rate, low power, power dissipation

1. Introduction

The operational amplifier (op-amp) is a core part in designing an analog electronic circuitry and mixed signal systems[1][2]. There are various levels of complexities when designing an operational amplifier and thus make it a versatile device that ranging from a dc bias generation to a high speed amplifications to filtering[3][4][5]. Operational amplifier is widely used in electronic devices today as it being used in industrial, scientific devices and in a vast array of consumer.

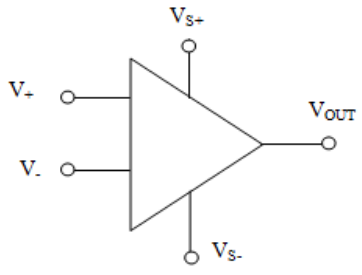

Figure 1. Symbol of op-amp

Op-amps is said to be a linear devices as it has nearly all the properties required for not only ideal DC amplification but also widely used for signal conditioning, filtering and performing mathematical operations such as additional, subtraction, differentiation, integration and etc[4][5]. A general operational amplifier consists of 3 terminal devices which two of it are inverting input represent by a negative sign ("-") and non-inverting

input represent by a positive sign ("+") and both of its have a very high input impedance. The third terminal of an operational amplifier is output port where it could be both sinking and sourcing either a voltage or a current. The difference between the two signals being applied to the two inputs of an operational amplifier is called the amplified output signal. Due to this, a differential amplifier is generally used as the input stage of an operational amplifier and hence an operational amplifier is also called a DC-coupled high-gain electronic voltage amplifier. Block diagram of an operational amplifier is described in Figure 2 where differential input amplifier is a first stage with two input voltage and common source stage as the second stage.

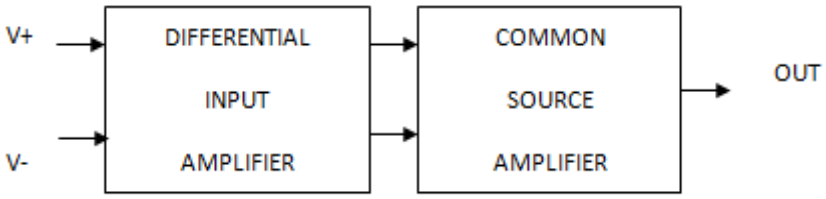

Figure 2. Block diagram of two-stage op-amp

A low power operational amplifier gives advantages in many applications owing to prolongation of battery life and thus makes it suitable for portable devices. In analog devices product development, it offers high power efficiency without compromising the speed, noise and precision. Low power op-amp is widely used as a bio-potential amplifier where it is used to amplify and filter extremely weak bio-potential signals[6]. In industrial sections, it is widely used in the usage of barcode scanner.

Nowadays, the need on smaller size chip with very small power dissipation has increased the demand on low power design. But the obstacles on designing a good performance of a low power op-amp are on operating with power supplies that is smaller than 1 Volt, on getting an ideal characteristic of op-amp specification and on designing a circuit with the same or better performance than circuits designed for a larger power supply.

This paper is organized as follows. Section II describes the proposed schematic design being considered. In Section III, the design method is presented. Section IV provides the simulation results, performance comparison, and discussions. Finally, our conclusions are given in Section V.

2. Proposed Schematic and Method

2.1 Proposed Schematic Two-Stage Op-Amp

The first block is an input differential amplifier and it was design to provide very high input impedance, a large CMRR and PSRR, a low offset voltage, low noise and also high gain [14-16]. The output is single ended so that the rest of the op-amp did not contain symmetrical differential stage and since the transistors is operating in the saturation region, there is an appropriate dc voltage difference between input and the output signals of the input stage.

Second block will perform level shifting, added gain and single to ended conversion. Level shifting is needed to compensate for dc voltage change occurring in the input stage so that an appropriate dc bias can be assured for the following stages. The added gain is used to provide gain or an additional amplification to the input stage as it is not sufficient. The conversion to single ended signal is performed in a subsequent stage as in some circuits, the input stage has a differential output.

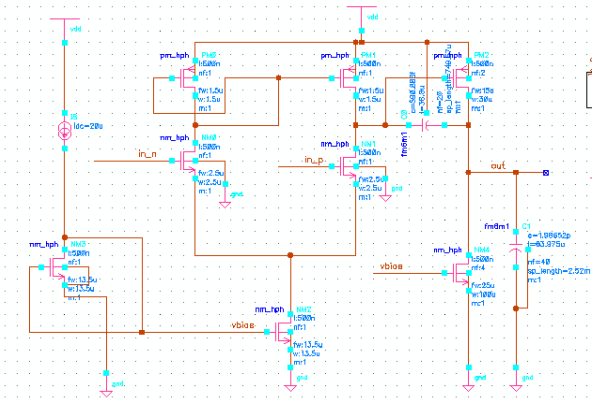

Figure 3. Proposed two-stage circuit design

2.2 Design Specification

Before start the design, there are several specification need to be assumed or take into consideration. The specifications are:

Table 1. Proposed design specification

Specifications	Proposed Value
Dc gain	1000/60dB
Phase margin	$\geq 60^{\circ}$
Slew rate	20V/μs
GBW	≥ 30MHz
ICMR +	1.6V
ICMR -	0.8V
CL	2pF
Power dissipation	≤400μW
V_{DD}	1.8V
Process	130nm

This consideration will be used to determine the width and length of the transistor. Based on the proposed schematic in Figure 3, the W/L ratio for M3 and M4 will be found from the max ICMR +, M1 and M2 will be found from the tranconductance gm1 and GBW, the current flow through M5 will be found from the slew rate, M5 and M6 will be found from minimum ICMR -, M6 from gain and the design of M3 and M4, I6 current flow to the second stage is related to the design of M3,M4 and I5, M7 is related to I5 because of the same biasing voltage and lastly the Cc value from phase margin. The length of the transistor value used when involving the two stage op-amp is L ≥ Lmin. Lmin is the technology used which is 130nm. So in this design the length used are either L=1000nm or L=500nm but only 500nm will be used. The 1000nm value will only be used if needed to satisfy the condition required. This large value is used to avoid channel length modulation and also the lambda, λ.

The op-amp has been design based on the given step below [7]:

2.3 Design Calculation

1. The length used is 500nm
2. The phase margin specification is 60°, so the compensation capacitor equation is

$$Cc \geq 0.22 \times CL \tag{19}$$

Cc is compensating capacitance and CL is the load capacitance.

3. The total current or the current flow through M5 is

$$I_5 = S_R \times Cc \tag{20}$$

4. Design of M1 and M2 from the gain bandwidth product (GBW) and the small signal transconductance from gate to channel (gm1)

$$\mathrm{gm1} = \mathrm{GBW} \times \mathrm{Cc} \times 2\pi \tag{21}$$

$$\left(\frac{\mathrm{W}}{\mathrm{L}}\right)1,2 = \frac{\mathrm{gm1}^2}{\mu\mathrm{ncox} \times \mathrm{I5}} \tag{22}$$

5. Design of M3 and M4 is from the maximum input common mode range (ICMR +)

$$(\mathrm{W/L})_{3,4} = \frac{\mathrm{I5}}{\mu\mathrm{pcox} \times [\mathrm{V_{DD}} - (\mathrm{ICMR_+}) - \mathrm{Vt3_{max}} + \mathrm{Vt1_{min}}]^2} \tag{23}$$

I5 is the drain current of M5, V_{DD} is the positive supply voltage, $ICMR_+$ is the maximum input voltage, V_t is the threshold voltage and µpcox is the transconductance parameter.

6. M5 and M6 design from the minimum input voltage range (ICMR-)

$$\mathrm{VDS5}_{SAT} \geq (\mathrm{ICMR} -) - \sqrt{[\mathrm{I_5}(\mu\mathrm{ncox}(\mathrm{W/L})_1)]} - \mathrm{Vt1_{max}} \tag{24}$$

$$(\mathrm{W/L})_5 = \frac{\mathrm{I_5}}{\mu\mathrm{ncox}(\mathrm{VDS5_{sat}})^2} \tag{25}$$

7. Design of M7 from gain and design related to M3 and M4

$$\mathrm{gm6} \geq 10 \times \mathrm{gm1} \tag{26}$$

$$(\mathrm{W/L})_6 = \frac{\mathrm{gm6}}{\mathrm{gm4}}(\mathrm{W/L})_4 \tag{27}$$

8. Design of M8 from the design of M3 and M4

$$\mathrm{I_6} = \frac{(\mathrm{W/L})6 \times \mathrm{I4}}{(\mathrm{W/L})4} \tag{28}$$

$$(\mathrm{W/L})_7 = (\mathrm{I_7} \times \mathrm{I_5}) \times (\mathrm{W/L})_5 \tag{29}$$

From all step above, the calculated value of different MOSFET is recorded in Table 3-2:

Table 2. Calculated Size of MOSFETs

Device	Type	Calculated Size
M1,M2	NMOS	2.5 µm /0.5 µm
M3,M4	PMOS	1.5 µm / 0.5 µm
M5,M6	NMOS	13.5 µm / 0.5 µm
M7	PMOS	30 µm / 0.5 µm
M8	NMOS	135 µm /0.5 µm
Cc	Load Capacitor	800f F

From Table 2, the size of M8 is optimized to 100µm so that the gain will increase while the value for Cc is optimized to 600fF so that the GBW will increase. Other parameters can also be varied such as if M1and M2 ratio increase, the gain, gm1 and GBW will also increase, then if deriving high maximum ICMR+ the M3 and M4 ratio need to be high, when determining a small value of ICMR- that closed to the ground the M5 and M6 ratio need to be very big. M7 and M8 contributed gain for the second stage so if it is decreased the overall gain will increase and lastly by decreasing the value of Cc the GBW value will increase as well. In this project design, only Cc and M8 are optimized

Table 3. Optimization Size of MOSFETs

Device	Type	Optimized Size
M1,M2	NMOS	2.5 µm /0.5 µm
M3,M4	PMOS	1.5 µm / 0.5 µm
M5,M6	NMOS	13.5 µm / 0.5 µm
M7	PMOS	30 µm / 0.5 µm
M8	NMOS	100 µm /0.5 µm
Cc	Load Capacitor	600fF

3. Result and Discussion

The design of two-stage op-amp was simulated based on its different characteristics such as transient, gain, GBW, phase margin, slew rate, CMRR, PSRR, output offset voltage and power dissipation. These characteristics are varied using ICMR of 0.8V and 1.6V. Furthermore, the layout of the designed op-amp was drawn. The different results are presented here.

3.1 Transient Analysis

An amplifier is an electronic device that modulates the output of the power supply. This analysis has been used to identify whether the output obtained is greater than the input of differential amplifier. The analysis has been done by connecting both input pair with sinusoidal voltage and dc voltage to V_{DD} and V_{SS} terminal. Figure 4 shows a plot of the two-stage op-amp output voltage V_O versus the differential input voltage in_n, in_p. The output obtained is 1.731V, in_p 990mV and -1.731V in_n -990mV.

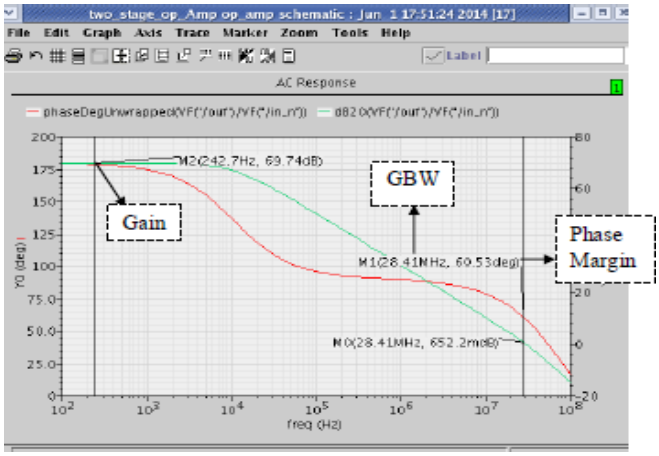

Figure 4. Transient analysis

3.2 AC Gain and Phase Analysis

This analysis has been done separately for ICMR + and ICMR -. From this analysis the gain, GBW and phase margin can be obtained. The gain is the ratio of the output to the input, GBW is the product of the bandwidth and gain at which the bandwidth is measured and the phase margin is measured to determine the stability of the design. For ICMR+, the gain obtained is 69.73dB, the GBW is 28.406MHz and the phase margin is 60.529. For ICMR -, the gain obtained is 76dB, the GBW is 28.406MHz and the phase margin is 60.252◦.

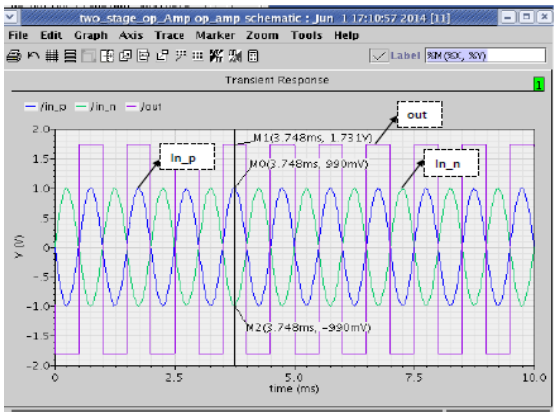

Figure 5. Op-Amp Gain for ICMR+

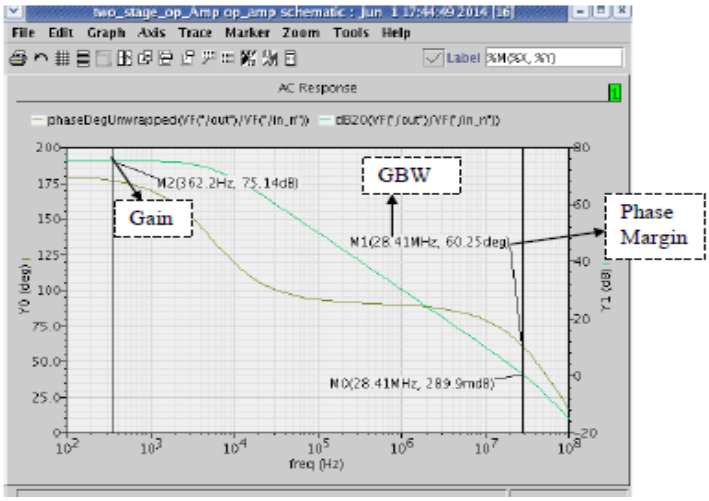

Figure 6. Op-Amp Gain for ICMR-

3.3 Input Common Mode Range (ICMR)

ICMR is the common mode voltage range. Usually the input-output transfer curve for ICMR simulation is linear and all MOSFETs are operated in saturation region. To measure the ICMR, the negative terminal of the first stage is connected to the output terminal and the positive terminal is connected to the dc voltage with frequency 1 kHz and DC voltage is swept from 0.8V to 1.6V with supply voltage VDD of 1.8V. The input common mode range of this two-stage op-amp slope is 0.982V which is approximately to 1V.

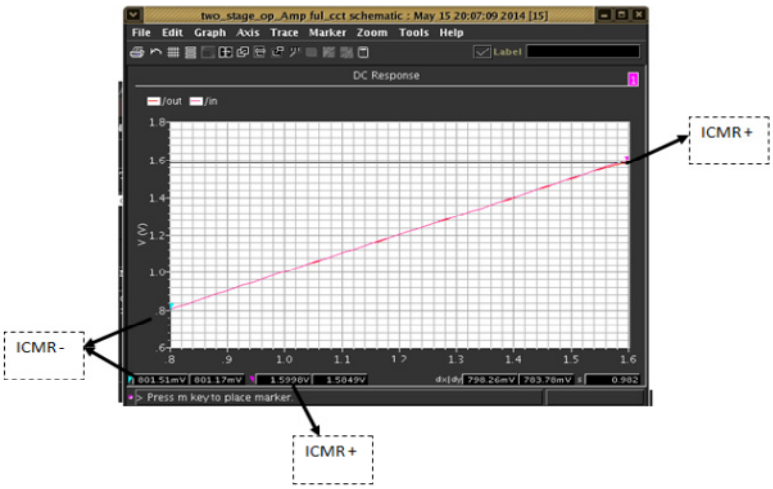

Figure 7. ICMR

3.4 Common Mode Rejection Ratio

CMRR analysis is used to measure how well a differential amplifier can reject the common mode input voltage that relative to the wanted difference signal. The value of CMRR is obtained by subtracting the differential mode gain with common mode gain. The CMRR values obtained is 62.93dB.

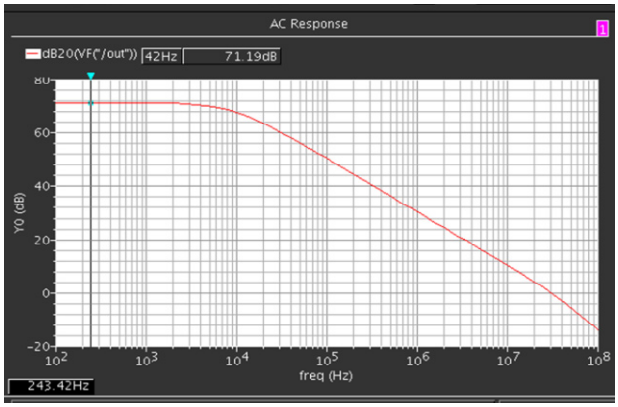

Figure 8. Differential Mode Gain

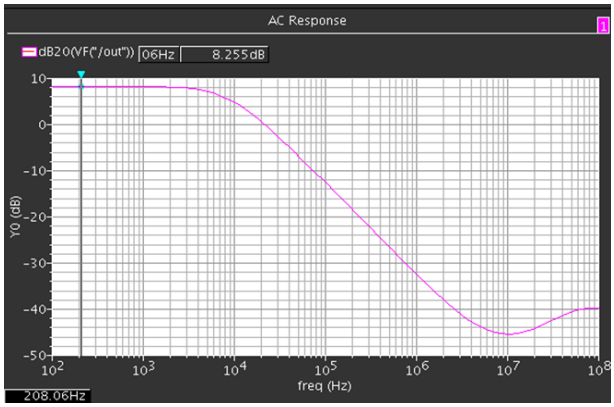

Figure 9. Common Mode Gain

3.5 Power Supply Rejection Ratio

PSRR analysis is used to describe the amount of noise from a power supply that a design op-amp can reject. PSRR is measured with both positive and negative power supply in decibel (dB). For PSRR + the VDD is supply with 1V amplitude, 1.8V of input voltage and 1kHz frequency while VSS is supply with -1.8V. Meanwhile, PSRR- is inversed from PSRR+. The input positive of differential amplifier is connected to the ground while input negative is connected to the output terminal. This condition is same for both PSRR. The PSRR + value obtained is 99.76dB and PSRR- value is 90.916dB.

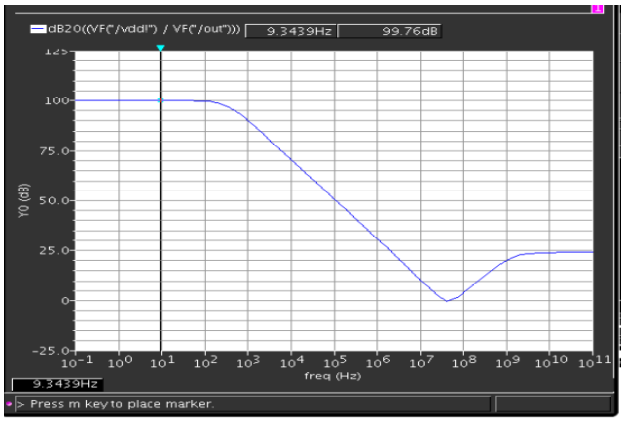

Figure10. PSRR+

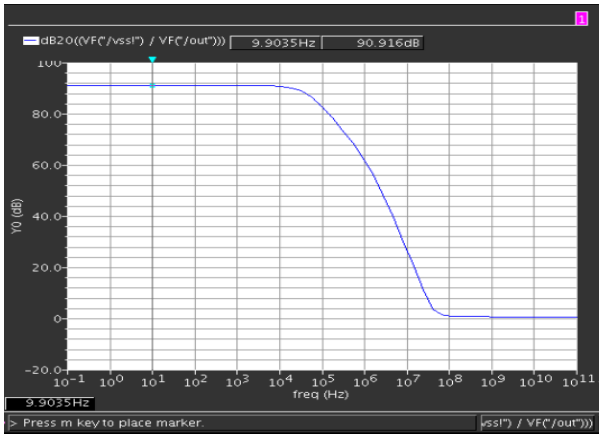

Figure 11. PSRR-

3.6 Slew Rate

Slew rate analysis is the maximum speed at which an op-amp can charge and discharge its load. Slew rate is measured by connecting input negative to output terminal and input positive is given a voltage pulse supply of 0.8V and 1.6V. The slew rate value is obtained on its rising and falling edge slope. The slew rate obtained is 20V/µs.

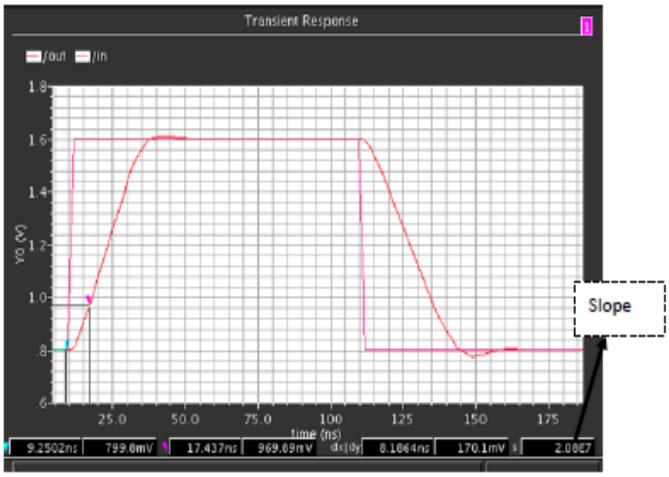

Figure 12. Rising Edge

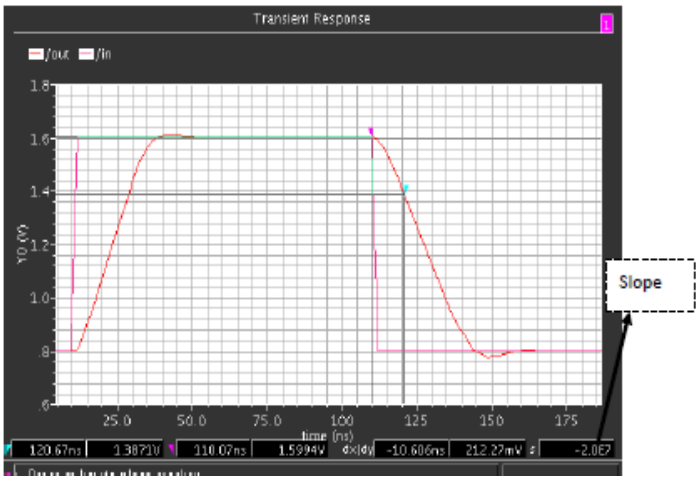

Figure 13. Falling Edge

Figure 14. Output offset voltage

3.7 Output Offset Voltage

When the input terminals are connected together, there is a voltage appears at the output of the differential amplifier called the output offset voltage. The output offset voltage value obtain is -1.5V

3.8 Power Dissipation

The power is calculated as the power dissipated by the VDD supply. In Cadence tools, this power dissipation is obtained by clicking the output tools then save all. After that at DC analysis save the DC operating points and done the simulation. The power dissipation value is then obtained by using the result browser. The power dissipation when ICMR+ is 0.3898mW and for ICMR – is 0.3644mW.

Table 4. Simulation result for low power op-amp

Parameters	Specification	Simulation Results
Gain	≥60dB	69.73dB
GBW	30MHz	28.406MHz
Phase Margin	≥60°	60.252°
Slew Rate	≥20V/µs	20.8V/µs
ICMR	0.8V-1.6V	0.8V-1.6V
CMRR	NA	62.93dB
PSRR	NA	99.76dB
Output Offset Voltage	NA	0V
Power Dissipation	≤0.4mW	0.389mW
Area	NA	2.44mm^2

4. Conclusion

An improved design and a comparative study of low power operational amplifier using a NMOS current mirror as bias circuit is presented in this research. The modified circuit has been designed by using the CADENCE 0.13-µm CMOS process. In this research, Designing of op-amps continues to pose further challenges as the supply voltages and transistor channel lengths scale down together with the introduction of each new generation of CMOS technologies. According to the research results, it has been proven that, the circuit is capable of providing a gain of 69.73dB and a 28.406MHz of gain bandwidth product for a load of 2pF capacitor. The results also verify that the modified circuit has CMRR of 62.93dB and output slew rate of 20V/µs. Moreover, the two-stage op-amp has a PSRR+ of 99.76 dB and PSRR- of 90.91dB. The presented op-amp has an Input Common Mode Range (ICMR) of 0.8V to 1.6V and power consumption of 0.389mW. Additionally, the circuit size reduced significantly by using small transistors and capacitors.

Acknowledgements

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Appendix A

Table A1. Work comparison

Work	**This work**	[8] 2013	[3] 2013	[9] 2013	[10] 2012	[11] 2012	[12] 2012	[5] 2011	[13] 2010	[17] 2008
Technology (µm)	**0.13**	0.6	0.18	0.18	0.18	0.1	0.18	0.18	0.8	0.35
Supply Voltage (V)	**1.8**	3.3	1.8	1.5	3	1.5	1.2	3	2	3.3
Gain (dB)	**69.73**	73.03	73.57	73.57	10.4	NA	79	20.14	61.1	72.6
GBW(MHz)	**28.4**	11.43	1.094	1.084	2.15	10	110	2.165	1.09	18.97
PM(deg)	**60.5**	50.4	65.86	65.89	93	60	60	NA	61	64
Slew Rate (V/µs)	**20.5**	5	NA	10.1	12.465	10	175	12.47	2.84	10
ICMR (V)	**0.8 – 1.6**	0.3-2.52	NA	0.143 -1.51	-1 - 2.4	NA	NA	-1 -2.4	0.16 -1.87	-1.54 -1.42
CMRR(dB)	**62.93**	51.5	147.9	147.9	64.4	NA	91	64	60.3	77.1
PSRR(dB)	**99.7**	109.3	88.84	92.95	86	NA	75	87	108	NA

Output Offset Voltage (mV)	**0**	NA	NA	NA	-603	0.75	0	-600	0.042	NA
Power Dissipation (mW)	**0.389**	1.23	4.35	3.54	1.18	450	3.34	0.6	0.0168	2.13
Area(mm^2)	**2.44**	NA	NA	NA	NA	NA	NA	NA	0.0084	NA

Appendix B

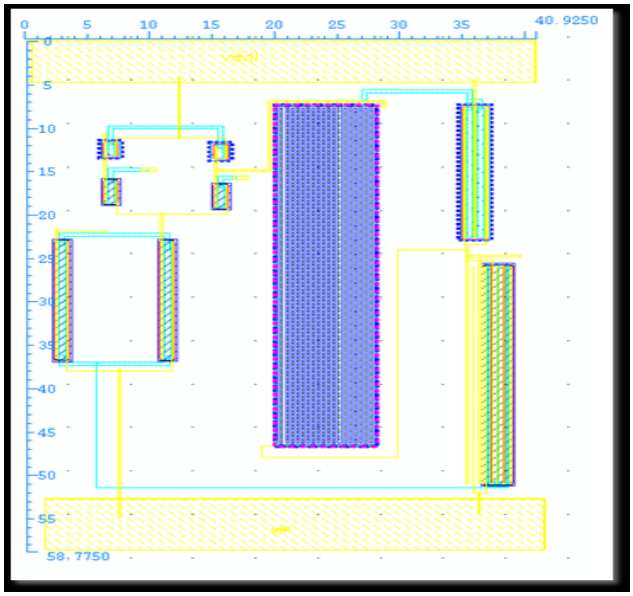

Figure B1. Layout of two-stage op-amp