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Efficiency Analysis of Low Power Class-E Power Amplifier

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Abstract

This paper presents an analysis of effect of inductor and switch losses on output power and efficiency of low power class-E power amplifier. This structure is suitable for integrated circuit implementation. Since on chip inductors have large losses than the other elements, the effect of their losses on efficiency has been investigated. Equations for the efficiency have been derived and plotted versus the value of inductors and switch losses. Derived equations are evaluated using MATLAB. Also, Cadence Spectre has been used for schematic simulation. Results show a fair matching between simulated power loss and efficiency and MATLAB evaluations. Considering the analysis, the proposed power amplifier shows about 13 % improvement in power effiency at 400 MHz and -2 dBm output power. It is simulated in 0.18 μm CMOS technology.

Keywords: low power, class e, power amplifier, efficiency analysis

1. Introduction

High efficiency and low level output power design of power amplifier (PA) is a requirement for optimization of the energy efficiency of the transmitter which is one the key building blocks of sensor nodes in wireless sensor networks. The class-E power amplifier can ideally achieve 100% efficiency. This high efficiency has spurred many research interests on the design and analysis of Class-E Pas (Apostolidou, et al, 2009; Lee, et al 2010; Brama, et al, 2008; Mertens, et al, 2002; Tsai, et al, 1999; Reynaert, 2006). The conventional class-E power amplifier can produce large power levels with good efficiency (Lee, et al 2010; Brama, et al, 2008; Mertens, et al, 2002. Most of the existing Class-E PA designs have been optimized to work at high output power levels, ranging from 23 to 33 dBm (Lee, et al 2010; Brama, et al, 2008; Mertens, et al, 2002; Tsai, et al, 1999; Reynaert, 2006; Mousa, 2013). If these fully integrated PAs are used in applications requiring low level output power such as wireless body sensor networks, the overall efficiency significantly degrades (Tan, et al, 2012). For example Bluetooth and ZigBee standards are short range standards that their output power level are from 0 to 10 dBm(Retz, et al, 2009; Eo,et al, 2007; Bae, et al, 2011) and in wireless body sensor networks it is even under 0 dBm (Cook, et al, 2006;Tan, et al, 2012). Therefore, high efficiency PA with low level output power is critical to short range wireless sensor network.

The efficiency of low power class-E power amplifier (LPCEPA) introduced by Jun Tan (Tan,et al, 2012) is appropriate for use in transmitter block of the sensor node in short range wireless sensor networks. LPCEPA architecture is a proper option for fully integrated PA solutions. Among the elements of a fully integrated design, on chip inductors have large losses than the others and have the most adverse effect on overall efficiency of the transmitter.

In this paper, to investigate the effect of inductor losses on LPCEPA efficiency, the equations of losses of elements and efficiency of PA vs. losses are derived and based on these observations an appropriate PA has been proposed.

The rest of this paper is organized as follows: In Section 2, the circuitry of the LPCEPA and circuit description is presented. Section 3 presents the analytical equations of the losses. In section 4, simulation results of the proposed PA are presented. Section 5 concludes the paper.

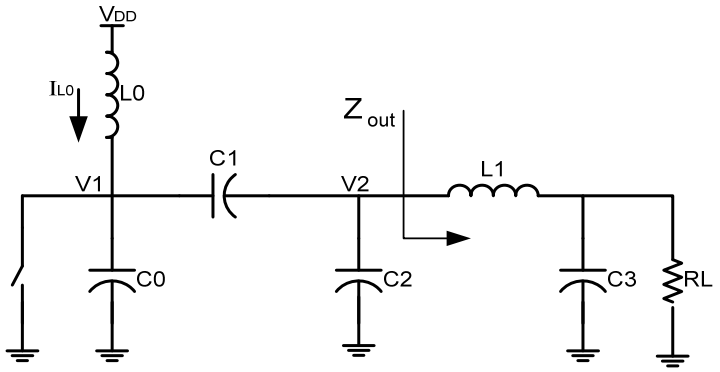

Figure 1. Schematic diagram of the LPCEPA

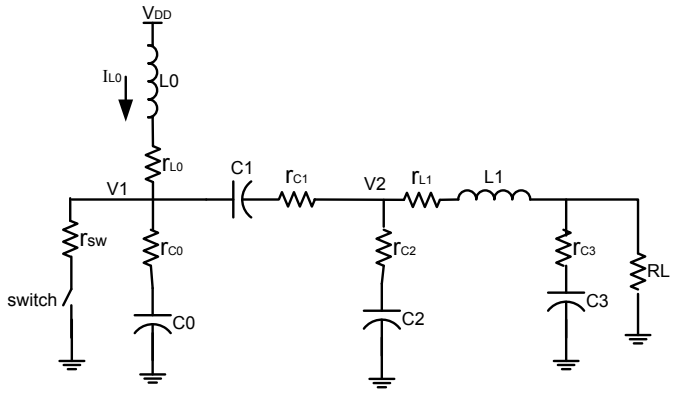

Figure 2. Schematic diagram of the LPCEPA with losses modelled as resistor

2. Circuit Description

With the following assumptions, the circuit model of LPCEPA shown in Figure 1 has been selected for evaluation. In the analysis of PA, except the resistor R_L, all of the elements are supposed to be ideal and the transistor is an ideal switch with zero and infinite resistance when turns on and off, respectively. Two equations define the class-E PA conditions, as below: (Apostolidou, et al, 2009; Lee, et al 2010; Brama, et al, 2008; Mertens, et al, 2002; Tsai, et al, 1999; Reynaert, 2006)

$$V_1(t_1) = 0, \qquad \frac{dV_1(t_1)}{dt} = 0 \tag{1}$$

where t_1 is the time that switch turns on.

This equivalent circuit consists of a switch shunt capacitance C_0, matching network and load resistor R_L. For the analysis, suppose that frequency of input signal, voltage of power supply and duty cycle are known variables. Unknown variables in the circuitry of Figure 1 are six variables; C_0, C_1, C_2, C_3, L_0 and L_1. To find unknown variables, six independent equations are required. Four new design variables are defined as:

$$C_{eq} = C_0 + \frac{C_1 C_2}{C_1 + C_2} \tag{2}$$

$$\alpha = C_1 / (C_1 + C_2) \tag{3}$$

$$\beta = C_0 / C_{eq} \tag{4}$$

$$q = 1 / (\omega_0 \sqrt{L_0 C_{eq}}) \tag{5}$$

where C_{eq} denotes the total capacitance at node V_1 , α is the ratio of C_1 to C_1+C_2, β is the ratio of parallel

capacitance C_0 to C_{eq} and q is the normalized frequency. The design challenge is to compute these four new variables. Once calculated, the value of the real elements C_0~C_2 and L_0 can be specified. The two variables I_a and φ are concluded next. When the switch is off, KCL equations at nodes V_1 and V_2 are:

$$C_1(\frac{dV_1(t)}{dt}-\frac{dV_2(t)}{dt}) = C_2\frac{dV_2(t)}{dt} + I_a\cos(\omega_0 t+\varphi) \tag{6}$$

$$i_{L0}(t) = C_0\frac{dV_1(t)}{dt} + C_1(\frac{dV_1(t)}{dt}-\frac{dV_2(t)}{dt}) \tag{7}$$

and the voltage drops across the inductor L_0 are as follows for the time switch is off and when it is on, respectively.

$$V_{DD} - V_1(t) = L_0\frac{di_{L_0}(t)}{dt} \tag{8}$$

$$V_{DD} = L_0\frac{di_{L_0}(t)}{dt} \tag{9}$$

When the switch is ON, node V_2 requires:

$$(C_1+C_2)\frac{dV_2(t)}{dt} = -I_a\cos(\omega_0 t+\varphi) \tag{10}$$

Solving differential equations, the waveform of V_1, V_2 and I_L when switch is off are:

$$V_1(t) = A_1V_{DD}\cos(\omega_1 t) + A_2V_{DD}\sin(\omega_1 t) + \kappa V_{DD}\frac{1}{q^2-1}\sin(\omega_0 t+\varphi) + V_{DD} \tag{11}$$

$$V_2(t) = \frac{C_1}{C_1+C_2}V_1(t) - \frac{I_a}{(C_1+C_2)\omega_0}\sin(\omega_0 t+\varphi) + A_3V_{DD} \tag{12}$$

$$i_{L_0}(t) = C_{eq}\omega_1[A_2V_{DD}\cos(\omega_1 t) - A_1V_{DD}\sin(\omega_1 t)] + \kappa V_{DD}C_{eq}\omega_0\frac{q^2}{q^2-1}\sin(\omega_0 t+\varphi) + V_{DD} \tag{13}$$

The variable κ is defined as:

$$\kappa = \frac{\alpha I_a}{C_{eq}\omega_0 V_{DD}} \tag{14}$$

For determining A_1, A_2 and κ, boundary conditions of voltage waveform V_1 can be used. The initial condition of V_1 is $V_1(0) = 0$. Solving the linear algebraic equations, the variables of A_1, A_2 and κ are:

$$A_1 = \frac{q(\sin(a_2)-\sin(a_1)+\sin(a_3)-\sin(a_4))+\sin(a_1)+\sin(a_2)}{q\sin(a_1)-q\sin(a_2)-2q\sin(\varphi)-\sin(a_1)-\sin(a_2)}. \tag{15}$$

$$A_2 = \frac{\sin(a_5)-\sin(\varphi)}{\sin(\varphi)\sin(a_4+\varphi)} - A_1\frac{\sin(\varphi)\cos(a_4+\varphi)-\sin(a_5)}{\sin(\varphi)\sin(a_4+\varphi)} \tag{16}$$

$$\kappa = \frac{-2q(q^2\cos(2q\pi(1-D))-\cos(2q\pi(1-D))-q^2+1)}{q\sin(a_1)-q\sin(a_2)-2q\sin(\varphi)-\sin(a_1)-\sin(a_2)} \tag{17}$$

and for the time interval that switch is on, V_1 is zero. Also, the current of inductor L_0 is:

$$i_{L_0}(t) = \frac{V_{DD}}{L_0}t + i_L(t_1) \tag{18}$$

By solving differential equation (10), V_2 can be calculated as:

$$V_2(t) = -\frac{I_a}{(C_1 + C_2)\omega_0}\sin(\omega_0 t + \varphi) + A_3 V_{DD} \tag{19}$$

to satisfy that all waveforms are periodic with the period of T, φ is:

$$\varphi = \tan^{-1}\left(\frac{k_2 + 2q\pi D k_3 - k_1}{-g_2 - 2q\pi D g_3 + g_1}\right) \tag{20}$$

The variables a_1, a_2, a_3, a_4, a_5, k_1, k_2, k_3, g_1, g_2 and g_3 used in equation above are given in the Appendix A. The output impedance Z_{out} at the first frequency can be computed by:

$$Z_{0ut} = (R_L \parallel \frac{1}{jC_3\omega_0}) + jL_1\omega_0 \tag{21}$$

Because V_2 is a periodic waveform, it can be expanded into its Fourier series. At the first frequency ω_0, Z_{out} is:

$$Z_{0ut} = \frac{V_{2\_1}}{I_a}\exp[(\varphi_1 - \varphi)j] = Z_{out\_real} + Z_{out\_imag} \tag{22}$$

V_{2_1} and φ_1 are amplitude and phase of the fundamental harmonic of V_2, respectively. From (21) and (22) equations, the C_3 and L_1 can be calculated.

With computing average current of L_0 inductor, consumption power can be calculated as below:

$$P_{DC} = V_{DD}^2 C_{eq} h \tag{23}$$

The variable *h* is given in the Appendix A

3. Analysis of Power Losses and Efficiency

In analysis of losses of LPCEPA, losses of elements are shown by a resistor in series with elements. Figure 2 shows the equivalent circuit of the power amplifier. The r_{L0} and r_{L1} are losses of the inductors L_0 and L_1, respectively. To simplify derivation of loss equations for inductors, root means square (RMS) current of L_0 inductor and maximum current of L_1 inductor are determined with suppose that currents of elements stay no changed when parasitic resistance are not zero.

The RMS current of inductor L_0 is:

$$I_{rms,L_0} = \sqrt{\frac{1}{T}\int_0^T i_{L_0}^2(t)dt} \tag{24}$$

and power loss in L0 inductor is determined by:

$$P_{loss,L_0} = I_{rms,L_0}^2 . r_{L_0} \tag{25}$$

For the time in which the switch is OFF (0<t<t1) iL0 is presented by equation 13 and for ON time of the switch it is given by equation 18. By integrating current from 0 to t_1 and from t_1 to T, $Irms,L_0$ can be calculated as:

$$I_{rms,L_0} = C_{eq}\sqrt{\frac{1}{T}(E_1 + E_2 + E_3 + E_4 + E_5 + E_6 + E_7)} \tag{26}$$

where variables E_1~ E_7 are given in the Appendix B.

Also, power loss in inductor L_1 is determined by:

$$P_{loss,L_1} = 0.5 I_a^2 . r_{L_0} \tag{27}$$

I_a is:

$$I_a = \frac{\kappa C_{eq} \omega_0 V_{DD}}{\alpha} \tag{28}$$

The current that flows through capacitor C0 is:

$$i_{C_0} = C_0 \frac{dV_1}{dt} \tag{29}$$

The RMS current of capacitor C_0 is given by equation 30.

$$I_{rms,C_0} = C_0 \sqrt{\frac{1}{T}(E_1 + E_2 + E_3 / q^4 + E_4 + E_5 / q^2 + E_6 / q^2)} \tag{30}$$

The power loss in shunt capacitor C_0 is shown in equation 31.

$$P_{loss,C_0} = I_{rms,C_0}^2 . r_{C_0} \tag{31}$$

Same procedure for capacitors C_1 and C_2 is done and equation for their current, RMS current and power loss are given by equations 32 ~ 37.

$$i_{C1} = C_1 (\frac{dV_1}{dt} - \frac{dV_2}{dt}) \tag{32}$$

$$I_{rms,C_1} = C_{eq} \sqrt{\frac{1}{T}(E_1 + E_2 + E_3 + E_4 + E_5 + E_6 + E_8)} \tag{33}$$

$$P_{loss,C_1} = I_{rms,C_1}^2 . r_{C_1} \tag{34}$$

$$i_{C2} = C_2 \frac{dV_2}{dt} \tag{35}$$

$$I_{rms,C_2} = \frac{C_1 C_2}{C_1 + C_2} \sqrt{\frac{1}{T}(E_1 + E_2 + E_3 / q^4 + E_4 + E_5 / q^2 + E_6 / q^2)} \tag{36}$$

$$P_{loss,C_2} = I_{rms,C_2}^2 . r_{C_2} \tag{37}$$

Considering Figure 2 the current flowing through C_3 can be calculated as:

$$I_{m,C_3} = I_a \frac{RC\omega_0}{\sqrt{(RC\omega_0)^2 + 1}} \tag{38}$$

And its power loss is:

$$P_{loss,C_3} = 0.5 I_{m,C_3}^2 . r_{C_3} \tag{39}$$

To calculate losses of switch resistance, its current must be known. When switch is open, its current is zero and when it's closed, its current is calculated using KCL in V_1 node as follows:

$$i_{sw} = i_{L0} - i_{C1} \tag{40}$$

and its RMS value is calculated by:

$$I_{rms,sw} = \sqrt{E_9 + E_{10} + Ceq^2 E_7 / T - C_1^2 C_2^2 E_6 / (q^2 (C_1 + C_2)^2 T)} \tag{41}$$

then, the losses of switch is:

$$P_{loss,sw} = I_{rms,sw}^2 . r_{sw} \tag{42}$$

Total power loss in the LPCEPA is the sum of power loss in inductors L_0 and L_1 and power loss in capacitances C_0~C_3.

$$P_{Loss} = P_{loss,L0} + P_{loss,L1} + P_{loss,C0} + P_{loss,C1} + P_{loss,C2} + P_{loss,C3} + P_{loss,sw} \tag{43}$$

Total power consumption is given by equation 23 and efficiency of the PA is:

$$\eta = \frac{P_{DC} - P_{loss}}{P_{DC}} \tag{44}$$

4. Simulation Results

The purpose of design of the LPCEPA is to be used in the transmitter of a short range wireless sensor network structure. Major advantages of LPCEPA are low level output power, high efficiency and on chip implementation of all elements. Since on chip inductors have large losses than the other elements, their effect on overall efficiency of PA has been discussed. To investigate the losses of on chip inductors in the PA, a schematic of LPCEPA (Figure 2) has been simulated with element values listed in Table1 using Cadence Spectre. Furthermore, equations governing this structure have been evaluated in MATLAB. In these simulations, only the losses of inductors and switch have been considered. Waveforms of the voltage of the drain terminal and the current of the inductor L_0 are shown in the Figure 3. Figure 4 shows the efficiency versus the losses of L_0, L_1 and switch when considered separately and together. Figure 5 shows the same for MATLAB evaluation.

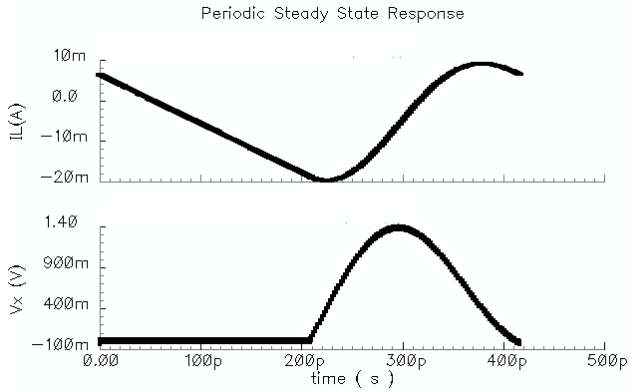

Figure 3. Waveforms of the drain node voltage and L_0 inductor current

Table 1. Simulation parameters and element values for simulated

Parameters & Elements	*Value*	*Unit*
L_0	3.3	nH
L_1	3.3	nH
C_0	240	fF
C_1	1	pF
C_2	1.3	pF
C_3	1.6	pF
R_L	50	ohm
Frequency	2.4	GHz
Duty cycle (D)	0.5	--
Power Supply	0.5	Volt

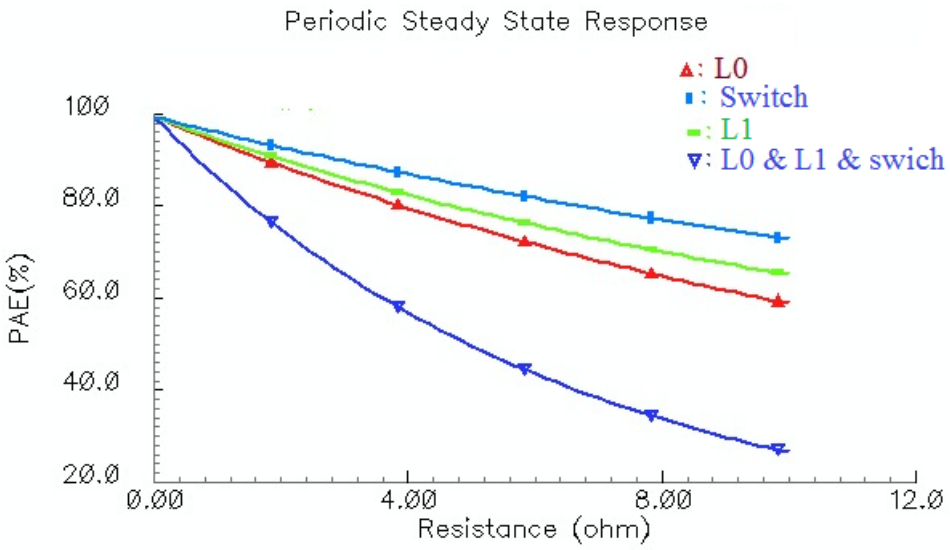

Figure 4. Efficiency of PA versus losses of inductors and switch (Cadence Spectre)

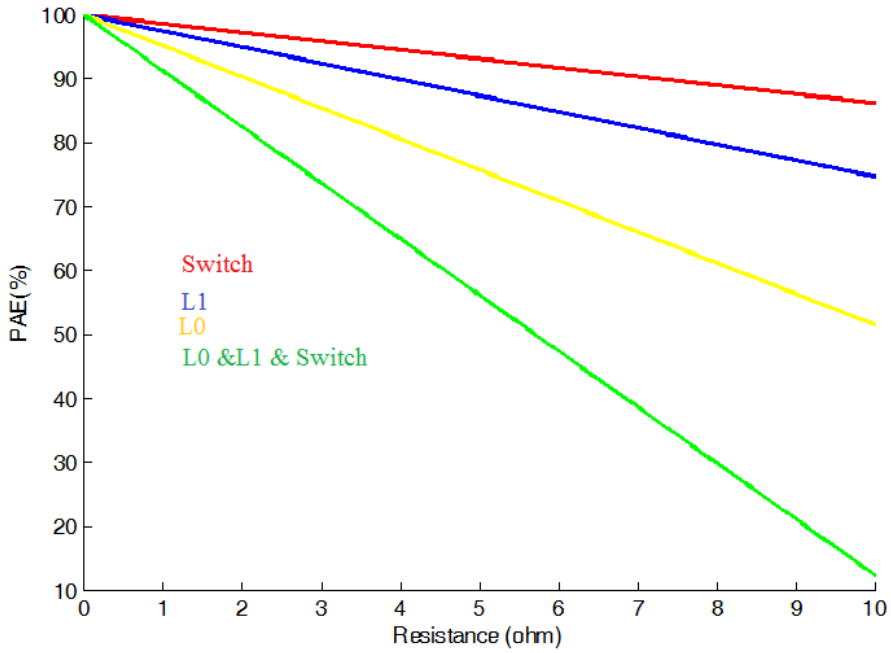

Figure 5. Efficiency of PA versus losses of inductors and switch (MATLAB)

Considering the efficiency analysis of the amplifier it can be concluded that to decrease the losses, output network can be changed such that the first harmonic RMS current does not pass through the inductor. To do this, we propose the following circuit. Simulation results for two structures show about 13 % improvement in efficiency.

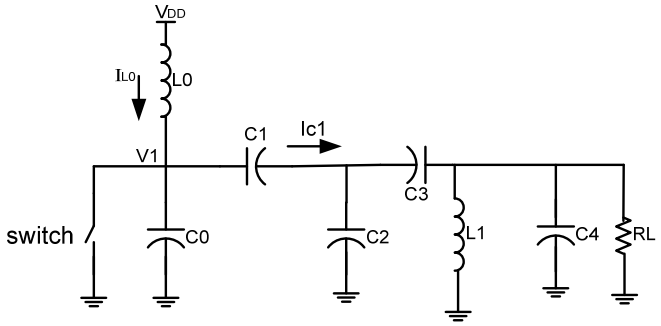

Figure 6. Proposed PA

To investigate the results, structures of Figure 1 and Figure 6 have been simulated using the component values listed in Table 2. PAE of both circuits versus series loss of inductors have been shown in Figure 8. For a 4-ohm series resistance, the difference in PAE of two circuits is 19%. Also, the analysis of both structures employing on chip inductors for -2 dBm output power at 400 MHz frequency shows that PAE of circuit LPCEPA (Figure 1) is 20% and that of circuit proposed PA (Figure 6) is 33%. Results are summarized in Table 3.

The proposed fully integrated amplifier for 400 MHz and -2 dBm has been shown in Figure 6. Component values are listed in Table 2. As supply voltage varies from 0.35 V to 0.6 V the output power varies from -3.1 dBm to 1.1 dBm (Figure 9).

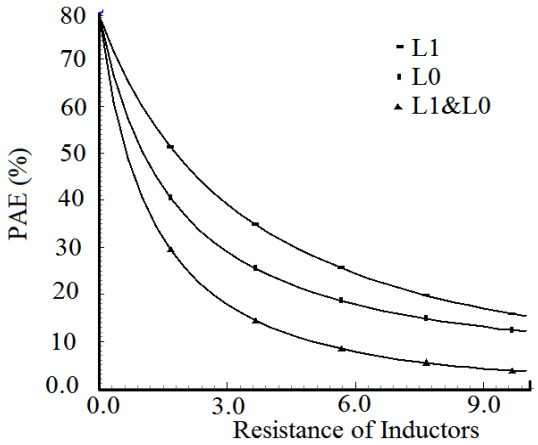

Figure 7. Efficiency of LPOCEPA versus losses of inductors (Cadence Spectre) with 2.4 GHz

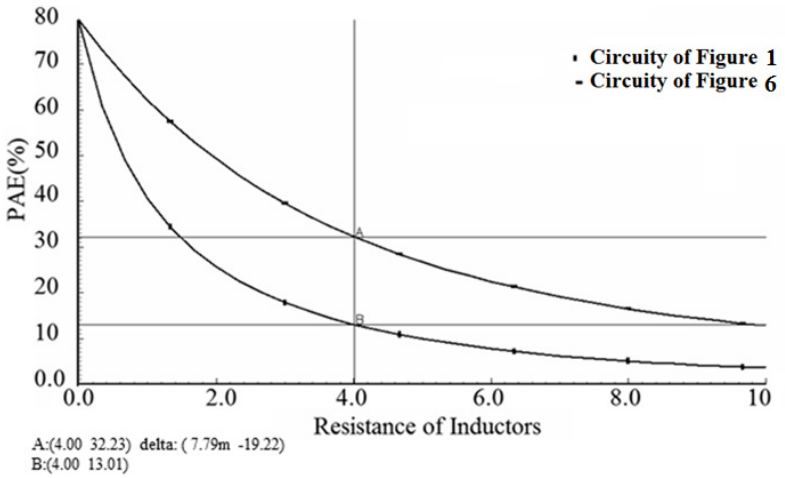

Figure 8. PAE of proposed PA Figure 5 and Figure 4 of circuit with losses of inductors

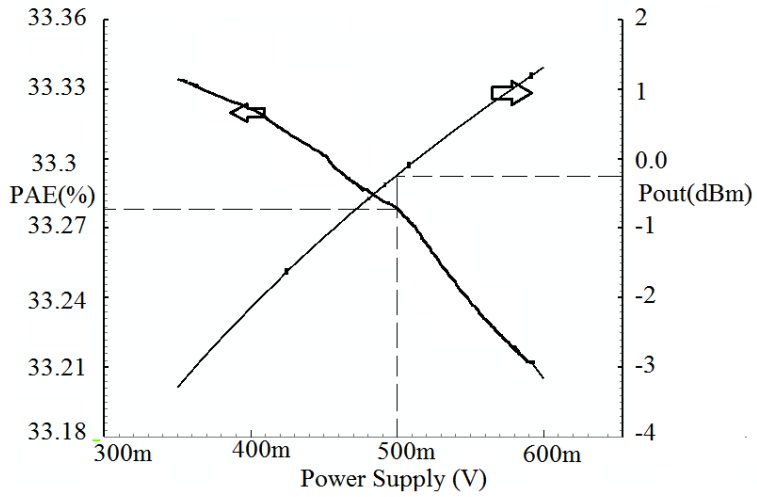

Figure 9. PAE and Pout of the proposed PA versus power supply

Table 2. Component value list for circuits of Figure 1 and Figure 6

Parameter	Circuitry of Figure 1		Circuitry of Figure 6	
Technology (μm)	0.18		0.18	
Power Supply	0.5 Volt		0.5 Volt	
Frequency	400 MHz		400 MHz	
Duty cycle	0.4		0.4	
Sub.	Inductors	capacitors	Inductors	capacitors
0	10.5 nH	1.65 pF	10.5 nH	4.2 pF
1	9.2 nH	5.52 pF	9.2 nH	9 pF
2	---	12.9 pF	---	12.9 pF
3	---	32.8 pF	---	40p
4	---	----	----	4p

Table 3. Results of the amplifiers of Fig. 1 and Fig. 6 for the component values listed in Table 1

	Frequency	**Pout**	**PAE**
Circuitry of Fig. 1	400(MHz)	-2 dBm	**20%**
Circuitry of Fig. 6	400(MHz)	-2 dBm	**33%**

5. Conclusion

In this paper, the effect of element losses on PA efficiency has been investigated. Since LPCEPA is suitable for fully integrated implementation and among the integrated elements on chip inductors have larger losses, equations for the efficiency have been derived and plotted versus the value of inductors losses. Results show that one of the inductors has larger contribution to the overall drop in efficiency. Derived equations are evaluated using MATLAB. Cadence Spectre has been used for schematic simulation. A fair matching between simulated power loss and efficiency and MATLAB evaluations can be seen from the plots. Considering the analysis, the proposed power amplifier shows about 13 % improvement in power efficiency at 400 MHz and -2 dBm output power level. The proposed PA is simulated in 0.18 μm CMOS technology.

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Appendix A

$$k_1 = -2q\sin(n_1)\sin(n_2) - 2\cos(n_2)\cos(n_1) - 2q^2(\cos(n_2)-1)(1-\cos(n_1)) + 2\cos(n_1) \quad (42)$$

$$k_2 = -2\cos(n_1) + 2\cos(n_2)\cos(n_1) \quad (43)$$

$$k_3 = 2q\sin(n_1)\cos(n_2) - 2\sin(n_2)\cos(n_1) \quad (44)$$

$$a_1 = 2\pi(1-D)(q+1) + \varphi \quad (45)$$

$$a_2 = 2\pi(1-D)(q-1) + \varphi \quad (46)$$

$$a_3 = 2\pi q(1-D) + \varphi \quad (47)$$

$$a_4 = 2\pi q(1-D) - \varphi \quad (48)$$

$$a_1 = 2\pi(1-D) + \varphi \quad (49)$$

$$g_1 = 2q\sin(n)(1-\cos(n_1)) - 2q^2(\cos(n_2)-1)\sin(n_1) + \sin(n_1)\cos(n_2) \quad (50)$$

$$g_2 = 2\sin(n_1) - 2\sin(n_1)\cos(n_2) \quad (51)$$

$$g3 = 2q\cos(n_2)\cos(n_1) - 2q + 2\sin(n_2)\sin(n_1) \quad (52)$$

$$n_1 = 2\pi(1-D) \quad (53)$$

$$n_2 = 2\pi q(1-D) \quad (54)$$

Appendix B

$$J_1 = q\omega_0 A_2 V_{DD} \quad (56)$$

$$J_2 = -q\omega_0 A_1 V_{DD} \quad (57)$$

$$J_3 = \kappa\omega_0 V_{DD}\frac{q^2}{q^2-1} \quad (58)$$

$$J_4 = \frac{1}{2q\omega_0}\sin(4\pi qD) \tag{59}$$

$$J_5 = \frac{1}{2q\omega_0}\sin(4\pi qD + 2\varphi) - \frac{\sin(2\varphi)}{\omega_0} \tag{60}$$

$$J_6 = \frac{1}{(q+1)\omega_0}\sin((q+1)2\pi D + \varphi) + \frac{1}{(q-1)\omega_0}\sin((q-1)2\pi D - \varphi) - \frac{2q}{(q^2-1)\omega_0}\sin(\varphi) \tag{61}$$

$$J_7 = -\frac{1}{(q+1)\omega_0}\cos((q+1)2\pi D + \varphi) - \frac{1}{(q-1)\omega_0}\cos((q-1)2\pi D - \varphi) + \frac{2q}{(q+1)\omega_0}\cos(\varphi) \tag{62}$$

$$E_1 = 0.5J_1^2(TD + J_4) \tag{63}$$

$$E_2 = 0.5J_2^2(TD - J_4) \tag{64}$$

$$E_3 = 0.5J_3^2(TD + J_5) \tag{65}$$

$$E_4 = \frac{J_1^2\ J_2^2}{q\omega_0}\sin^2(2\pi qD) \tag{66}$$

$$E_5 = J_1^2 J_3^2 J_6 \tag{67}$$

$$E_6 = J_2^2 J_3^2 J_7 \tag{68}$$

$$E_7 = \frac{V_{DD}}{3L_0^2}(1-D)^3T^3 + i_{L_0}^2(t_1)(1-D)T + \frac{V_{DD}}{L_0}i_{L_0}(t_1)(1-D)^2T^2 \tag{69}$$

$$E_8 = \frac{T}{2}(1-D) + \frac{1}{4\omega_0}(\sin(\varphi) - \sin(4\pi D + 2\varphi)) \tag{70}$$

$$E_9 = kC_{eq}V_{DD}i_{L0}(t_1)[\sin(\varphi) - \sin(2\pi D + \varphi)]/\pi/\alpha \tag{71}$$

$$E_{10} = -C_{eq}^2\ V_{DD}^2\ \kappa\omega_0[2\sin(\varphi) - 2D\sin(2\pi D + \varphi) - \cos(\varphi)/\pi + \cos(2\pi D + \varphi)/\pi] \tag{72}$$