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Design of a Low Voltage Schmitt Trigger in 0.18 μm CMOS Process With Tunable Hysteresis

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Abstract

Schmitt triggers are commonly used in communication and signal processing techniques to solve noise problem. A low voltage Schmitt trigger circuit with tunable hysteresis is proposed in this paper. For obtaining hysteresis under low voltage, a cross-coupled static inverter pair is used. By adjusting the symmetrical load operation, the hysteresis of the Schmitt trigger is varied. The cross-coupled inverter pair regenerative operation is controlled by it. Designed in 0.18 μm CMOS process technology, the simulation results show that the proposed Schmitt trigger circuit's triggering voltage can be adjusted approximately 0.5 V to 1.2 V. The proposed design is suitable to be implemented in buffers, sub-threshold SRAMs, retinal focal plane sensors, wireless transponders and pulse width modulation circuits.

Keywords: CMOS, comparator, Schmitt trigger, tunable hysteresis

1. Introduction

Schmitt Trigger circuit is widely used in analogue and digital circuits to increase noise immunity (Akter et al., 2008a, b; Reaz et al., 2007a, b; Marufuzzaman et al., 2010; Reaz et al., 2003; Reaz et al., 2005). It converts a varying voltage into an unvarying logical voltage signal (zero or one). The DC transfer characteristics are the major distinction in Schmitt trigger and comparator. For negative going and positive going input signals, Schmitt trigger has various switching thresholds known as hysteresis. Schmitt trigger does not respond if input signal noise magnitude is lesser than switching threshold variation. As such, it is resistant to noise (Saini et al., 2009; Kulkarni et al., 2007; Wu & Chiang, 2004; Liu et al., 2000; Kim et al., 2007). Buffers, sub-threshold random access memory, retinal focal plane, sensors, wireless transponders, pulse width modulation circuits etc use the Schmitt trigger circuits (Reaz et al., 2006; Reaz & Wei, 2004; Mohd-Yasin et al., 2004; Mogaki et al., 2007).

Conventional operational amplifiers based Schmitt triggers suffer from high power consumption and op-amp design challenges. Researchers exploited the potential benefits of CMOS technology for designing the Schmitt triggers (Allstot, 1982; Chen & Ming-Dou, 2005; Dokic, 1984; Katyal et al., 2008; Kim et al., 1993; Kosasayam, 2004; Kuang & Chuang, 2001; Niklas & Yiannos, 2012; Pedroni, 2005; Zhang et al., 2003). The most commonly quoted single ended Schmitt trigger was proposed by Dokic (1984). Dokic's design piles 4 transistors in between ground and power rails. Thus, the design is not suitable for low voltage applications. Chen and Ming-Dou (2005) proposed a Schmitt trigger based on design of Dockie. The proposed circuit functioned under a 3.3 V without high-voltage-gate-oxide over stress. By using a multilayer Schmitt trigger, larger voltage variation between two switching threshold voltages was attained (Kuang & Chuang, 2001). However, the design needed the four transistors stack in between ground and power rails. Thus, it was not suitable for low voltage applications.

Device dimensions, process parameters and supply voltages determine hysteresis. Kim et al. (1993) used 10 transistors in his proposed Schmitt trigger design for forming required regenerative feedback. Al-Sarawi (2002) also proposed a low-power CMOS Schmitt trigger. Pedroni et al. (2005) proposed ultra-low-voltage Schmitt trigger utilizing the body biasing technique. By adding an extra active pull up path, two switching threshold voltages can be simply attained. A logical threshold voltage control circuit proposed by Kosasayam et al. (2004) by setting the logical threshold. But the variable channel size MOS transistors required a careful mask design for logical threshold voltage control circuit. However, the logical threshold voltage can also be tuned in the narrow

range. Katyal et al. proposed a Schmitt trigger based on the design of Kid et al. (Katyal et al., 2008; Kim et al., 1993).

This paper presents a low voltage Schmitt trigger with tunable hysteresis that utilizes a cross-coupled static inverter pair for obtaining hysteresis under low voltage. The proposed Schmitt trigger hysteresis is varied by controlling the symmetrical load that regulates the cross-coupled inverter pair's regenerative operation.

2. Conventional Schmitt Triggers

Schmitt trigger is like a comparator which includes positive feedback. The output is high for an input higher than a chosen threshold level. On the hand, the output is low if the input is lower than a threshold. The output retains the value if the input is within these two. The conventional Schmitt trigger circuit and transfer curve are shown in Figure 1.

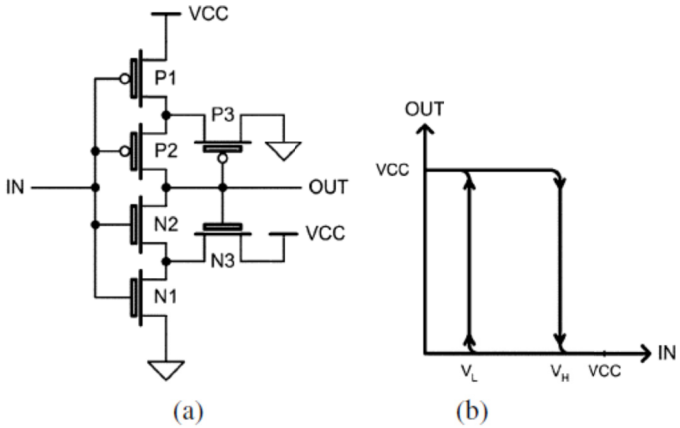

Figure 1. (a) Conventional Schmitt Trigger Circuit, (b) Voltage Transfer Curve

Hysteresis determined by the device supply voltages, dimensions and process parameters are the general disadvantage of the previously mentioned Schmitt triggers. As such, hysteresis varies with process conditions. The parameters spread have to be tolerated from batch to batch as well as from chip to chip.

3. Proposed Low Voltage Tunable CMOS Schmitt Trigger

The schematic of the proposed low voltage tunable CMOS Schmitt trigger is illustrated in Figure 2. To improve the tunable load currents and linearity of V/I characteristics, symmetrical loads are employed. The symmetrical loads act like voltage-controlled current sources set by Vc1, Vc2 and impedances set by the M3 and M4 mainly. The M3, M4 width is set much smaller than M5, M6 such a way that M5, M6 sets the current source impedance. The width of M7-M10 widths are set much smaller than M1-M2, M5-M6 such a way that the latch formed by the M7-M10 can be reset by the input Vin. The respective transistor dimensions are shown in Table 1.

Table 1. The transistor dimensions

NMOS Transistor	W/L (μm)	PMOS Transistor	W/L (μm)
M1–NMOS	10/0.18	M3–PMOS	5/0.18
M2–NMOS	10/0.18	M4–PMOS	5/0.18
M7–NMOS	2.5/0.18	M5–PMOS	20/0.18
M8–NMOS	2.5/0.18	M6–PMOS	20/0.18
M11–NMOS	10/0.18	M9–PMOS	5/0.18
M14–NMOS	20/0.18	M10–PMOS	5/0.18
M1 –NMOS	20/0.18	M12–PMOS	20/0.18
		M13–PMOS	20/0.18

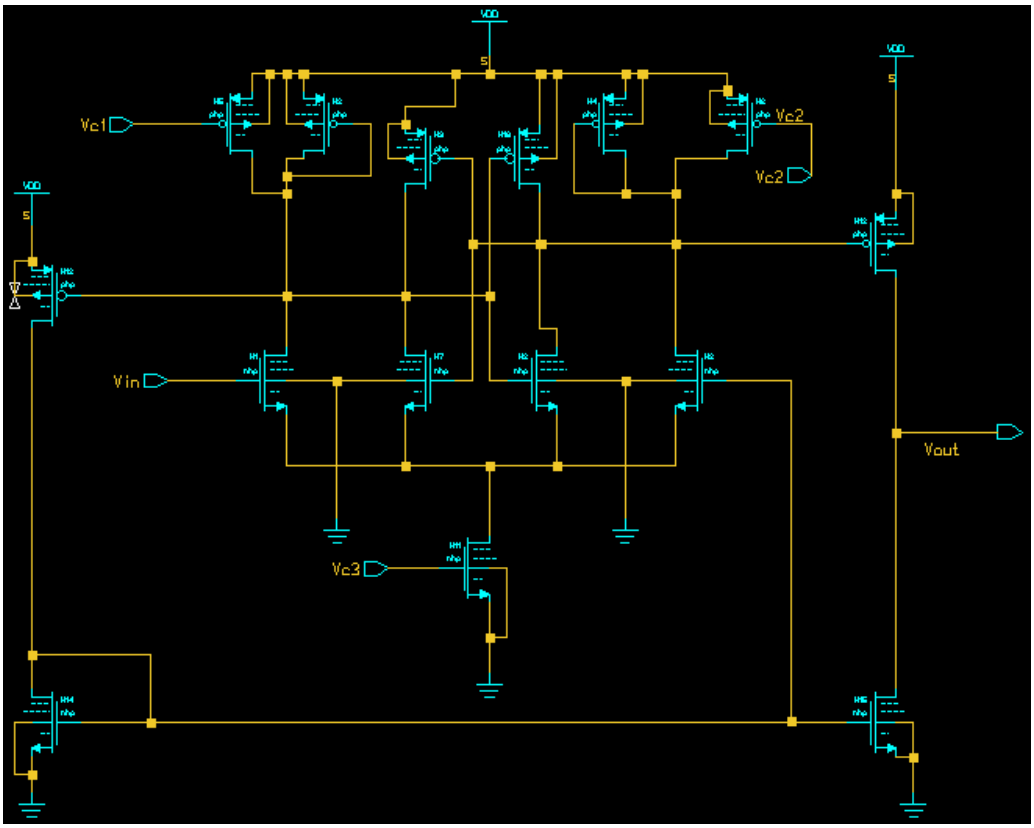

Figure 2. Schematic of proposed low voltage tunable Schmitt Trigger

4. Results and Discussions

The Schmitt trigger was designed using Silterra's 0.18 µm fabrication standard under 0.8 V CMOS technology and analyzed by simulation using CEDEC's Silterra Design Kit for Mentor Graphics software. Figure 3 shows the waveform at pMOS M12 where Vss is approximately 0.17 V. When there is logic 0 at M12, M4, M7 and M9 are off and M1, M2, M5, M6 and M8 are in the saturation state.

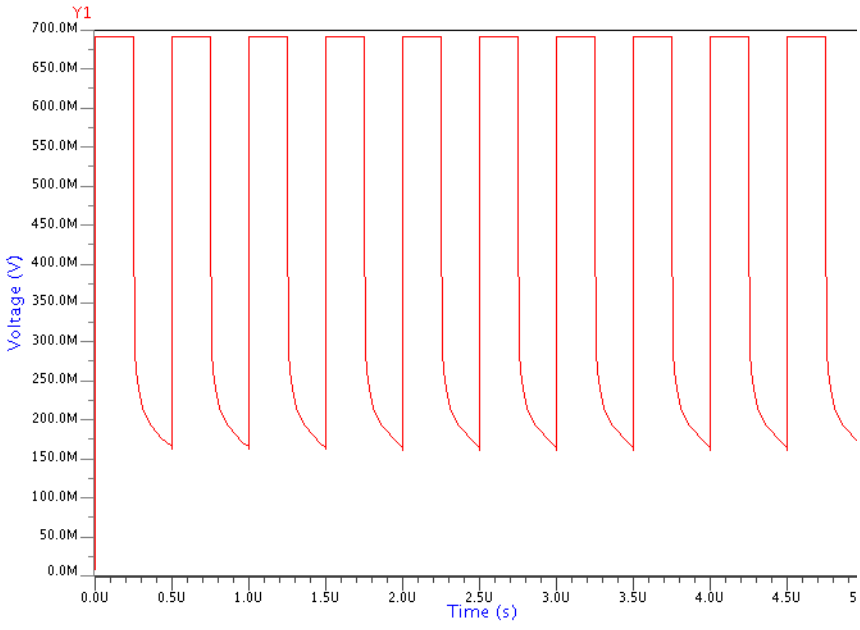

Figure 3. Output waveform at PMOS M12

The simulation results of input/output are shown in Figures 4, 5 and 6 for three different levels of voltage tested and simulated i.e. 0.8 V, 1.0 V and 1.8 V. The discrete triggering voltages are evident.

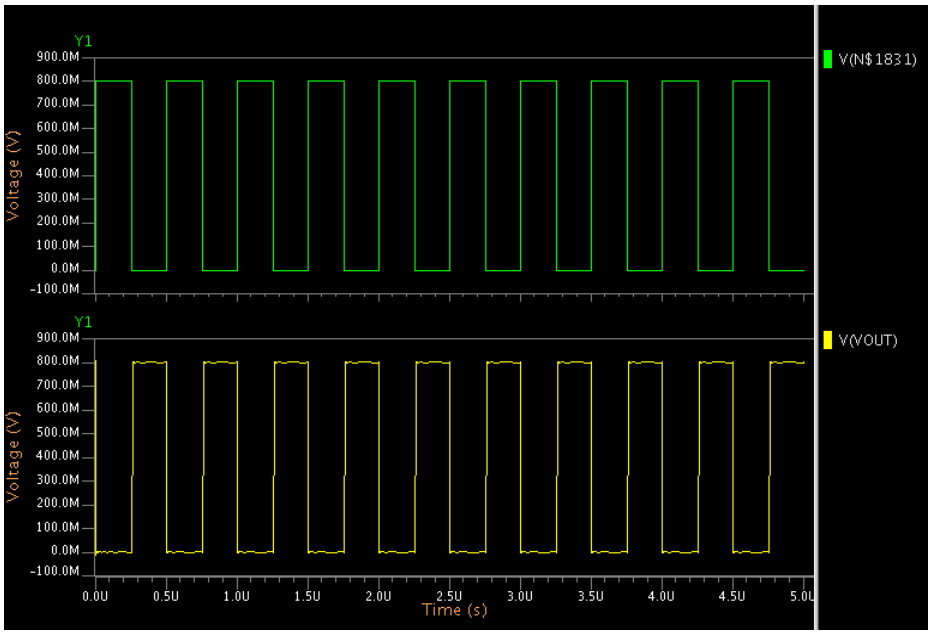

Figure 4. Simulation snapshot input/output waveforms at 0.8 V

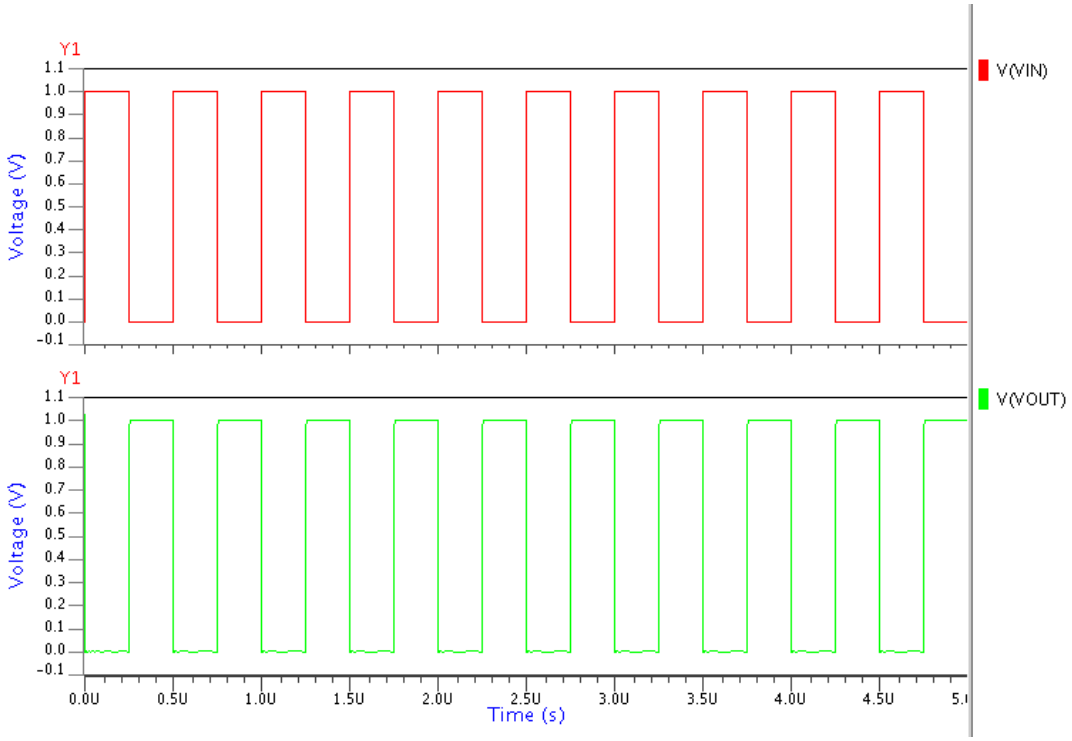

Figure 5. Simulation snapshot input/output waveforms at 1.0 V

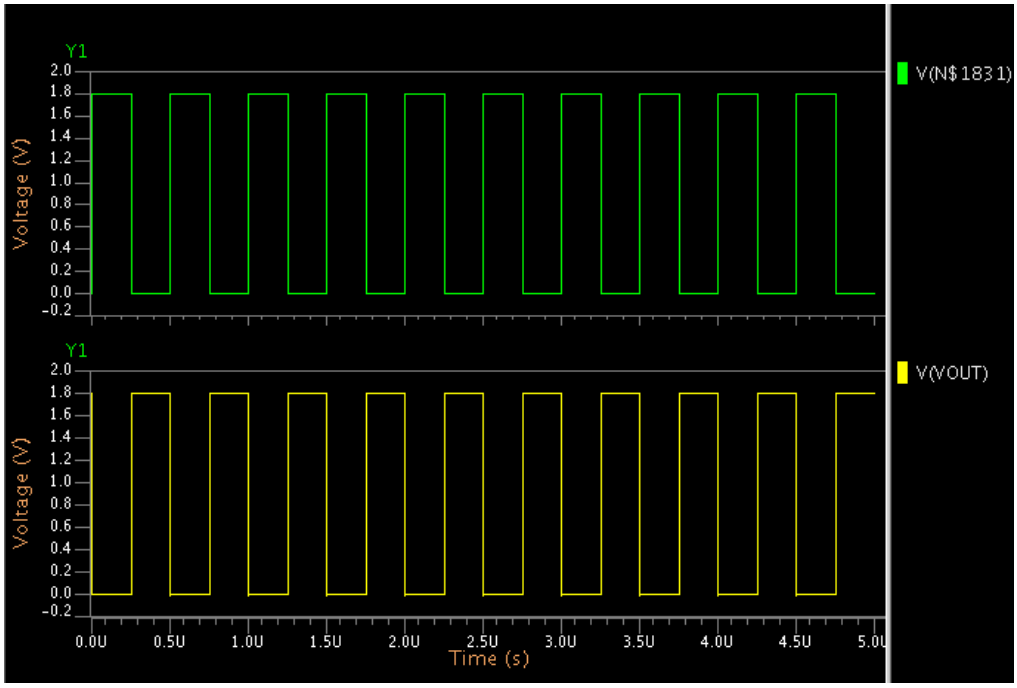

Figure 6. Simulation snapshot input/output waveforms at 1.8 V

The proposed Schmitt trigger DC voltage transfer characteristics with 2 different level of voltages are shown in Figures 7 and 8. It is seen that the state transition occurs when inverter pair is not activated. When the inverter pair is activated, the hysteresis exists and state transition gets sharper, owing to regenerative effect.

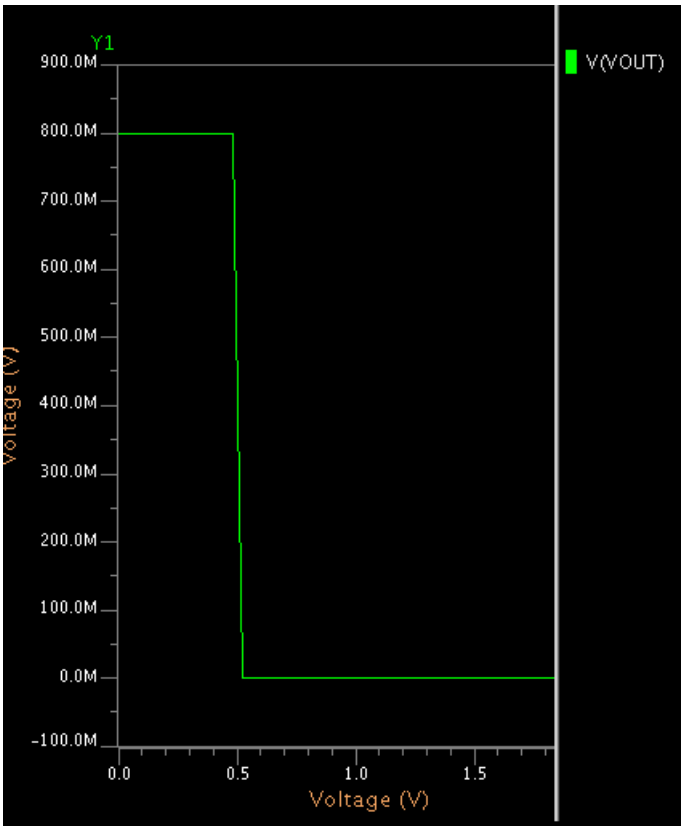

Figure 7. DC voltage characteristics at 0.8 V

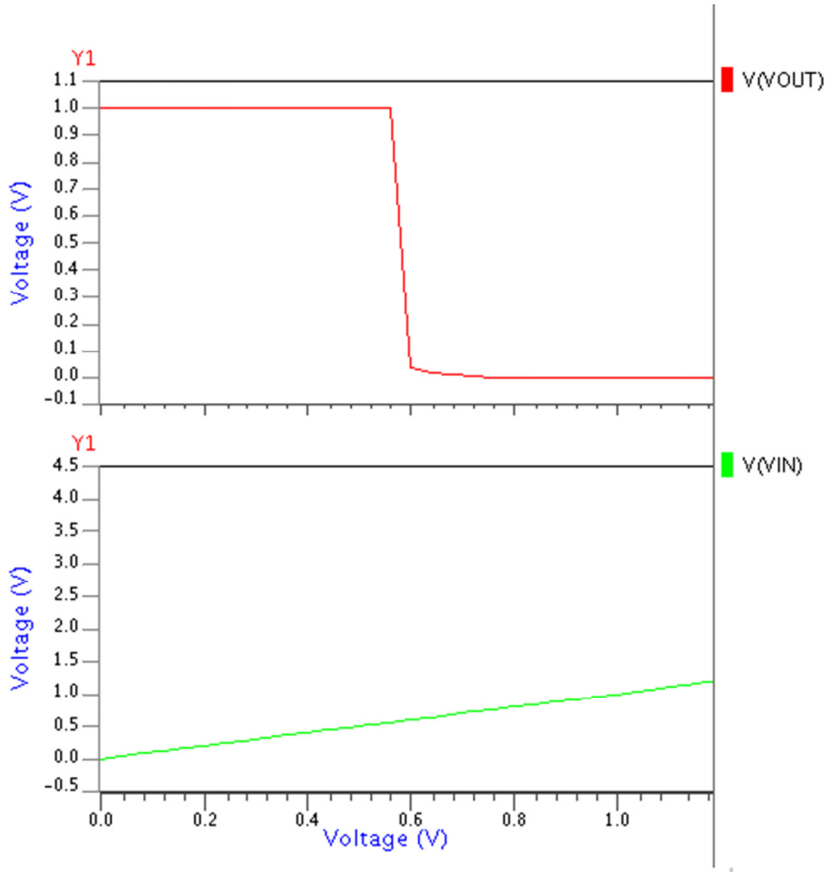

Figure 8. DC voltage characteristics at 1.0 V

It is perceived that proposed Schmitt trigger's triggering voltage can be varied approximately from 0.5 V to 1.8 V. But in between 0.5 V to 0.8 V there will be some spikes in output. The good results can be taken at 1.0 V to 1.2 V with very less spikes at 1.8 V. The power consumption is 189.1838 µW only.

A comparisons study of voltage and technology used for Schmitt Trigger implementation is illustrated in Table 2. From the table it is evident that proposed Schmitt trigger can work between 0.5 V to 1.2 V that lesser than the reported.

Table 2. Comparison of voltage and technology

Research	Vdd	CMOS Technology
Pedroni, 2005	3.3 V	0.5 µm AMI
Pham, 2007	3.0 V-3.3 V	0.5 µm AMI
Kim and Kim, 2007	0 V-0.7 V	0.15 µm BSIMSOI3.2
This Work	0.5 V-1.2 V	0.18 µm CEDEC

The layout of the proposed Schmitt trigger is drawn by using the CEDEC's Silterra Design Kit for Mentor Graphics at 0.18 µm standard process. The layout design is shown in Figure 9.

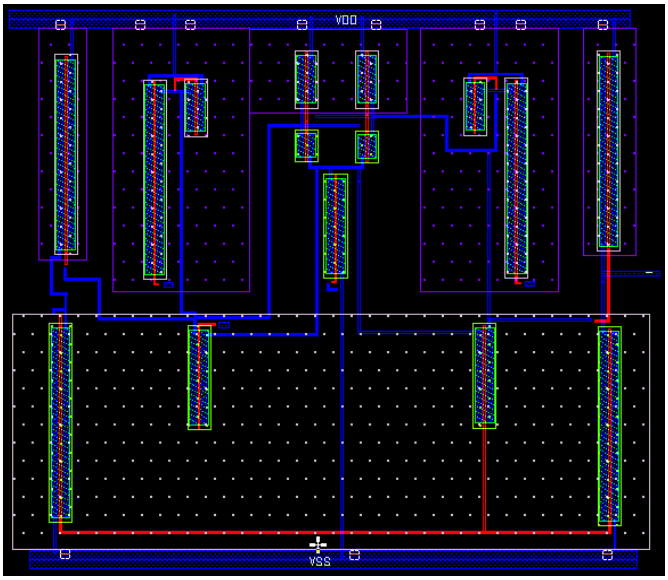

Figure 9. Layout of the proposed Schmitt Trigger

5. Conclusion

A Low Voltage tunable hysteresis CMOS Schmitt trigger is proposed in this paper. The design has advantages of low power and tunable hysteresis operated under low voltage which can vary from 0.5 V to 1.8 V. The system simulation result at 0.8 V with temperature setting of 27 °C is found satisfactory. The system is suitable to be implemented in buffers, sub-threshold SRAMs, retinal focal plane sensors, wireless transponders and sensors and pulse width modulation circuits.

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