

The Implementation of CAN Bus Adapter Based on CH372

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Abstract

To implement quick and reliable communication between CAN bus network and computer, we propose a sort of design method of CAN bus network adapter based on CH372, and mainly introduce the concrete implementations of hardware circuit and software program in this article. This system adopts the modularization design, and a new USB interface chip CH372 is adopted in the USB communication module, which can simplify the design of software program. SJA1000 bus controller is adopted in the CAN bus module. The system can effectively implement the data transfer between CAN bus and computer with high speed.

Keywords: USB bus, CAN bus, CH372, SJA1000

1. Introduction

In the CAN bus measurement and control network, the network adapter assumes the important task of data transfer between monitor unit and lower computer. The design of traditional adapter is generally based on ISA bus and EISA bus, which has not fulfilled the need of high-speed data transfer nowadays. Though the network card based on PCI bus has quick transfer speed, but it still has many disadvantages and deficiencies such as complex agreement, system resource occupation, nonsupport hot swap and expensive price. Though RS232 has convenient swap, but its transfer speed is too low, and its maximum communication speed is only 20Kbps. USB bus supports hot swap, and it is easy to be extended, and it has quick speed, so it is the ideal choice to design CAN bus adapter. However, past USB interface chips always adopt PDIUSB12 and USBN903, and their software designs were complex. In this design, we adopt new USB interface chip CH372 with interior integrated USB agreement, which could make program design and implementation easier, and users could put their energies on the design of application. The adapter designed in this article is actually applied in the product updating project of Tianjin Dantai S&T Development Co. Ltd. The practice proved that the design could enhance the communication speed, its installation and maintenance were convenient and it had extensive application future in the industrial control domain.

2. The implementation of adapter hardware circuit

2.1 Total structure of hardware circuit

The hardware circuit of the adapter designed in this article adopts the modularization design including main controller module, USB bus communication module and CAN bus communication module. The main controller module adopts AT89C51, and it mainly complete the initialization works of CH372 and SJA1000, and the communication tasks of USB bus and CAN bus. The total structure of CAN bus network adapter is seen in Figure 1.

2.2 Hardware design of USB communication module

The hardware circuit of USB bus communication module adopts new-style agreement chip CH372, which could not only simplify the design of hardware circuit, but reduce the design of software program. The SCM AT89C51 mainly completes the initialization work to CH37, responds the interrupt produced by CH372, and completes the data transfer with computer. The hardware circuit of USB bus communication module is seen in Figure 2.

CH372 is a full speed USB interface chip, and it is compatible with USBV2.0, and it supports plug and play, and its surrounding electron components only include crystals and capacitances.

CH372 has all-purpose local 8bits data bus and 4 lines control including read strobe, write strobe, chip selection input and interrupt output. The WR# and RD# of CH372 could respectively connect with WR# and RD# pins of SCM. CS# connects with P2.1 of SCM. The interrupt level outputted by INT# is that the low level is effective, and it is connected to INT0 of SCM. A0 is the address line input, and it differentiates order and data port, internally installs weak pull-up resistance, and when A0=1, it could write order, and when A0=0, it could read and write data. In the design, A0 connects with pin P2.0 of SCM. So the I/O addresses on the write order port of CH372 could be defined as 0xBD00, and the I/O addresses on the read and write data port could be defined as 0xBC00. When WR# is on high level and CS#, RD# and A0 are on low level, the data in CH372 output through D0-D7, and when RD# is on high level and CS#, WR# and A0 are on low level, the data are written in CH372 through D0-D7, and when RD# is on high level and CS# and WR# are on low level and A0 is on high level, the orders are written in CH372 through D0-D7.

CH372 internally installs power supply POR, so it generally needs not reset from the exterior. CH372 needs 12MHz clock signal supplied by the exterior when it works normally. The clock signals are produced by the inverter internally installed in CH372 through crystal stabilized oscillator. The surrounding circuit only needs to connect a crystal with standard frequency of 12MHz between XI and XO, and the pin XI and pin XO respectively connect with a high frequency oscillator capacitance. CH372 supports 5V power supply voltage or 3.3V power supply voltage. When it works on 5V voltage, VCC pin of CH372 inputs exterior 5V power supply, and the V3 pin should exteriorly connect with the decoupling capacitance of about 0.1μF. When it works on 3V voltage, V3 pin of CH372 should connect with VCC pin, and input exterior 3.3V power supply, and the work voltage of other circuits connected with CH372 should not exceed 3.3V.

2.3 Hardware design of CAN communication module

The hardware circuit of CAN bus communication module adopts CAN bus control chip SJA1000, bus driver PCA82C250 and high-speed photocouplers 6N137. The SCM AT89C51 completes the initialization of SJA1000, and implements the transmission and acceptance of data through controlling SJA1000. The hardware circuit of CAN bus communication module is seen in Figure 3.

CAN controller adopt SJA1000 made by PHILIPS, and it could work on BasicCAN mode or PeliCAN mode. The maximum bit speed could achieve 1Mbit/s, and it supports Intel and Motorola microcontroller. SCM could interview SJA1000 through the mode to interview exterior memorizer.

WR#, RD# and ALE of SJA1000 respectively connect with WR# and RD# of SCM. The pin INT# of SJA1000 connects with INT1 of SCM. The patch selection port of SJA1000 connects with P2.3 of SCM, and the low level is effective, and its initial address is defined as 0xBB00. TX0 and RX0 of SJA1000 connect with CAN bus transceiver PCA82C250 through high-speed light-coupler insulation 6N137. To avoid the collision of over current, CANH and CANL of PCA82C250 respectively connect with CAN bus through 5Ω current limited resistance. CANH and CANL parallel connect two 30pF capacitances with earth, which could eliminate the high frequency interference and prevent certain electromagnetic radiation on the bus.

3. The implementation of adapter software program

3.1 Total structure of software circuit

The software program in the design mainly includes USB communication module software program, CAN communication module software program and upper computer software program.

3.2 Software design of USB communication module

CH372 internally integrates the bottom agreement in USB communication, and it possesses convenient internal firmware mode and flexible exterior firmware mode. Under the internal firmware mode, it shields relative USB agreements, and automatically completes standard USB enumeration collocation process, and largely simplifies the firmware programming of SCM without any disposal to local port controller.

Because CH372 doesn't deal with complex bottom communication agreement, so it is very simple to design the software program for USB communication module. The programs mainly include the initialization of CH372 and the interrupt disposal program. The initialization program of CH372 mainly includes USB work mode setting, USB firmware mode (interior firmware or exterior firmware) setting, and exterior custom USB VID and PID setting.

CH372 is specially used to deal with USB communication, and it informs SCM to deal with the data by the interrupt mode after it receives data or transmits data. The interrupt disposal program mainly includes the disposal to patch download success, the disposal to patch upload success, and the disposal to upload interrupt data success. The interrupt disposal flow is seen in Figure 4.

The interrupt program first acquires interrupt status and cancels interrupt request and judges the types of the interrupt, which mainly include three types such as patch ports download success, patch ports upload success and interrupt data transmission success, then makes out different disposals according to the interrupts with different types, and if the

interrupt is induced by the patch ports download success, it also should make out disposal after judging whether the download is data or order.

3.3 Software design of CAN communication module

The functions of the physical layer and the link layer of CAN bus are completed by SJA1000, and the software program in the design mainly includes SJA1000 initialization subprogram, message transmission subprogram and message acceptance subprogram, and the disposals to data overflow interrupts and frame errors.

The initialization of SJA1000 could be implemented only under the reset mode, and the initialization mainly includes the setting of work mode, the setting of acceptance protection register AMR and acceptance code register ACR, the setting of baud rate parameter, and the setting of interrupt allowance register IER. The basic transmission process is that AT89C51 saves data to SJA1000 transmission buffer, and then resets the transmission require TR symbol of order register and begins to transmit. The acceptance process is that SJA1000 stores the data received from the bus to the acceptance buffer, inform AT89C51 to deal with the received information through the interrupt symbol bit, empties the buffer after acceptance and waits for receiving next time. The acceptance flow is seen in Figure 5.

3.4 Program design of the upper computer

For the program design of upper computer program, CH372 offers the interface of application layer. The interface of application layer is the API facing function application offered by CH372 DLL, and all APIs will return operation status after transfer, but answer data do not certainly exist, which could largely simplify the program design of the upper computer. APIs offered by CH372 DLL include equipment management API, data transfer API and interrupt disposal API. User program could transfer corresponding API function according to actual needs.

4. Conclusions

The CAN bus network adapter designed in the article combined the advantages of CAN and USB, and it extends the function application of USB in the industrial control. The system has many advantages such as good real time performance, high reliability and easy implementation, and it could implement the high-speed data communication between computers and CAN bus in the product testing of Tianjin Dontai S&T Development Co. Ltd, so it possesses good application foreground.

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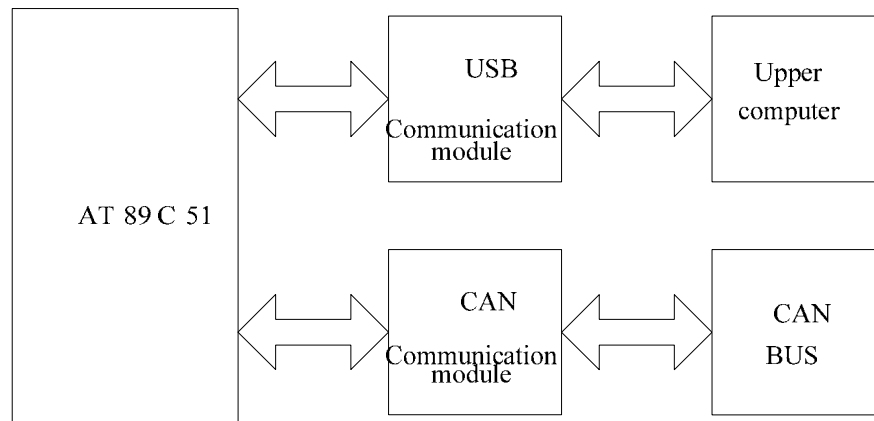


Figure 1. The Sketch of CAN Bus Network Adapter

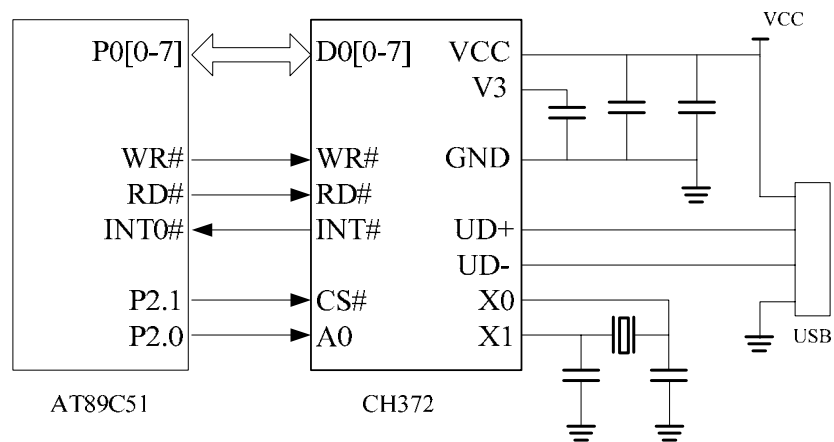


Figure 2. The Hardware Circuit of USB Bus Communication Module

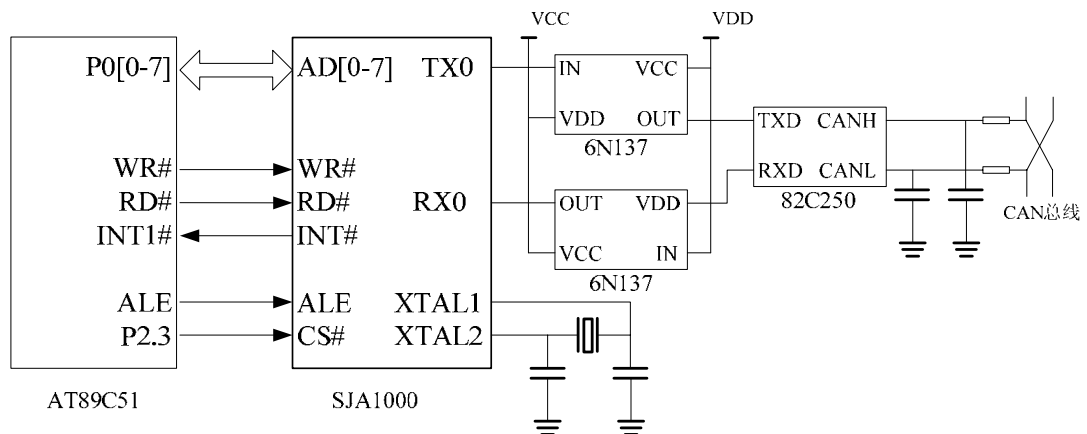


Figure 3. The Hardware Circuit of CAN Bus Communication Module

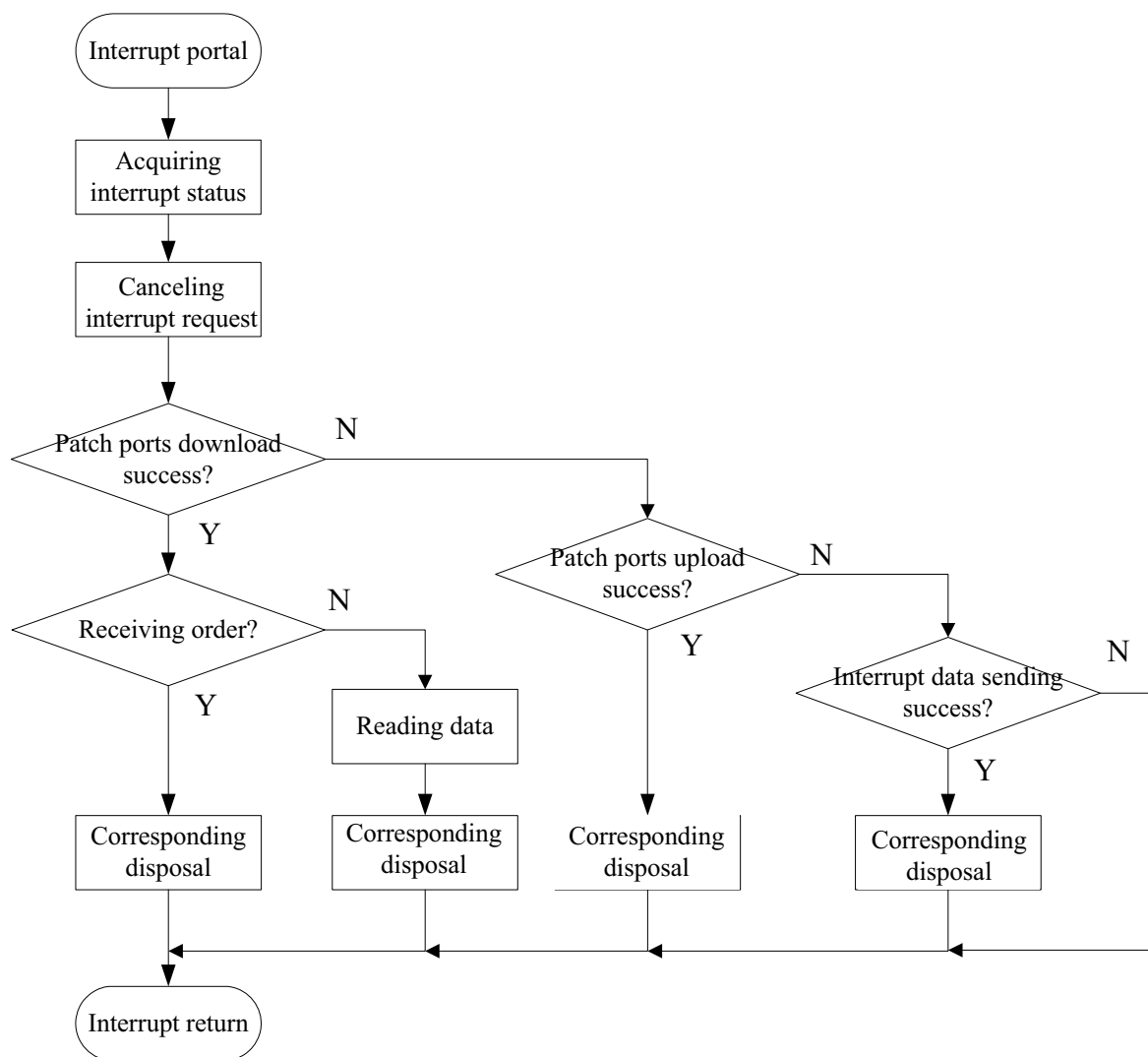


Figure 4. CH372 Interrupt Processing Flow

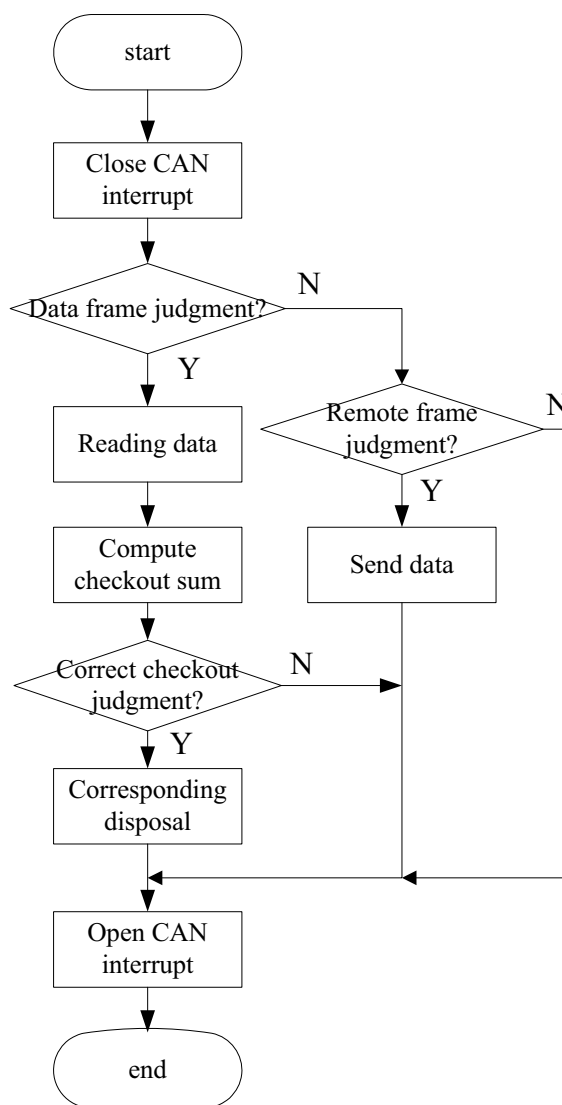


Figure 5. CAN Communication Module Acceptance Flow