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Simulation and Analysis of Fully Adiabatic Circuit Designing with Single Power Clock for High-Frequency Low-Power VLSI Circuits

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Abstract

Adiabatic logic guarantees vast diminishments of power utilization since it doesn't disperse power. This paper audits ongoing advancements in adiabatic circuits. First, the fully adiabatic circuit designing technology called pass-transistor adiabatic logic (PTAL) is discussed. Next, the operation of the dual-rail logic and the power clock supply with the logic operation of the PTAL technology is discussed. Further, many basic logic circuits using the PTAL technology are designed, compiled, and simulated. Finally, the performance results, power dissipation, speed, efficiency, and load analysis of the circuits are compared with the conventional and existing CMOS technologies under the same simulation conditions using standard 45nm technology with VDD = 1V and prove that even at high frequencies above 2GHz, it can outperform the dominating conventional CMOS logic designing in the field of power dissipation. The simulation results are provided to support our claim. We used 45nm technology for all our simulations.

Keywords: adiabatic circuit, pass-transistor logic, nano-electronics, low-power VLSI, high-speed IC, power clock

1. Introduction

As the demand for portable devices such as laptops and cell phones grows, so does the need to reduce their power consumption. Traditional methods such as voltage scaling are slowly reaching their limits, making it increasingly difficult to achieve these stringent power needs, especially as system complexity grows. It is now more important than ever to use non-conventional and logical methods to reduce power use. One of the prominent approaches to address this existing issue is to use fully adiabatic circuits. In this approach, we apply some thermodynamic principles to electrical circuits (Shinghal et al., 2013; Rabaey et al., 2012; B. Voss et al., 2001; Swami Y et al., 2016). It is feasible to transmit energy between two heat sinks while only losing a minute amount of energy if the energy transfer is purposefully delayed in thermodynamics. Similarly, if charge transfer in electrical circuits occurs at a far slower rate than the natural RC, we dissipate very little power. The quantity of power dissipated is directly proportional to the rate of charge transfer (Bhuvana et al., 2019; Swami Y et al., 2019a; T. Indermauer et al., 2002; Swami Y et al., 2017).

In the surge of the nano-electronics industry, we have been encountering a remarkable spurt in development, because of the utilization of IC design in data computations, media communications, and customer electronics. From the period of the first transistor in 1958 to modern ULSI designs with millions of transistors in a single chip, we've come a long way. In recent decades, the expanding number of transistors fabricated and synchronized on a chip, as well as the increasing transistor switching speed, has empowered incredible execution and performance change in IC frameworks. Shockingly, such amazing execution changes and enhancements have been followed by a rise in framework power consumption. High energy-power consumption characteristics in extra-efficient frameworks necessitate more expensive bundling, fabrication, and cooling improvements, resulting in cost increment and lower framework reliability quality.

The key driving force for the improved performance has been the advanced digital CMOS IC logic and circuit architecture. It motivates nano-electronics advancements for a variety of scientific and technological applications. The demand and interest in digital CMOS nano-chip design will continue to develop in the future due to its critical excellent upgrades and characteristics, such as high speed, low power, consistent execution, and improvements in fabrication and processing technology. In any event, when performance and execution demand rise, the level of on-chip integration and clock frequency will rise as well. The increased performance

framework's power usage and energy consumption will be a major design constraint (A. Blotti et al., 2004; Hu J et al., 2005; Kumar A et al., 2021; Roy K et al., 2009).

Integrated circuits' advanced features and applications have created a demand for low-power nano-electronic circuit design. The Intel 4004 CPU, released in 1971, had 2300 transistors and a clock frequency of 1 MHz. It had a power dissipation of around 1 watt. The 2001 Pentium, which has 42 million transistors and operates at a 2.4 GHz clock speed, uses around 65 watts of electricity in total. The reducing size of integrated circuits causes power density to increase exponentially while power dissipation increases linearly over time. A computer would have the same power as a nuclear reactor if the exponential rise in power density kept up. Due to reliability difficulties including electro-migration, thermal stresses, and hot-carrier effects that result in device deterioration brought on by the high power density (MOSIS, n.d.; Swami Y et al., 2018; C. HU, 2014; Swami Y et al., 2019b; W. J. Zhang et al., 2010). This contributes to the performance decline even further. The expanding market for battery-operated portable consumer gadgets is another factor boosting demand for low-power integrated circuits. Indirectly, low power consumption translates to the need for electrical products that are more compact, lighter, and durable. Battery life is gradually taking centre-stage in portable systems. For these systems, low power consumption is crucial since it directly affects performance by shortening battery life. In this environment, low-power VLSI design has become well-known as an active and rapidly developing field. Hence, in portable and battery-operated systems, a low-energy operation is essential. Therefore, in this manuscript, we try to explore the key sources of power/energy dissipation; and propose a PTAL technology with corresponding logic to reduce power/energy dissipation. The recommended advanced low-power PTAL technology outcomes are supported by the simulation results. The proposed model outcomes are compared with conventional CMOS technology and validated using the TCAD circuit simulator at the 45nm technology node.

2. Adiabatic Circuit Design

Semi-adiabatic and truly adiabatic circuits are two different types of adiabatic circuits. In contrast to truly adiabatic circuits, which in ideal situations have no un-adiabatic power dissipation at any level, semi-adiabatic circuits contain some un-adiabatic power dissipation at each stage of the adiabatic pipeline. The 2N2N-2P circuit logic style is an excellent illustration of the former, whilst split level charge recovery logic is a good illustration of the latter (SCRL).

It should be noted that the SCRL circuit design style, despite the lack of un-adiabatic power dissipation, they have numerous drawbacks as compared to the 2N2N-2P circuit logic design. It requires more power clocks and a greater area due to the presence of reversible power pipelines. Hence, we use the 2N2N-2P circuit logic style in designing our models. We could observe that the development of adiabatic logic, as a method of reducing the energy consumption of digital logic, has succeeded in achieving the limits to some extent. It makes efficient use of ac power supply to recycling the energy utilized to charge the node-capacitances of the logic circuits. Even though various innovative techniques have been developed, each including many creative ideas, there are several flaws in those circuits. The flaws can be listed as; the logic implementation is extremely complicated (Shinghal et al., 2013; Rabaey et al., 2012; B. Voss et al., 2001; Swami Y et al., 2016; Bhuvana et al., 2019). The need for several power-clock supplies is necessary for efficient stage-to-stage interface, hence the logic gates are not well suited for CMOS implementation. The non-adiabatic transitions may jeopardize the energy savings.

The proposed pass-transistor CMOS adiabatic logic (PTAL) is a dual-rail semi-adiabatic logic that uses only one power clock supply and has a comparatively low gate complexity (two-phase). In terms of performance and energy consumption, the simple implementation of PTAL outperforms previously disclosed adiabatic logic families.

3. Fully Adiabatic PTAL Operation

PTAL is a four-stage trapezoidal power-clock (PC) that supports dual-rail logic with pass-transistor NMOS functional blocks of F and $\bar{F}$, as well as a pair of cross-coupled PMOS devices in each stage. The PTAL four stages can be listed as evaluate-stage, hold-stage, discharge-stage, and idle-stage. During the Evaluate (E) stage, the PC is rising and evaluating the logic output. Hold (H) stage, the evaluated logic output is held at the respective logic level with the PC at its peak. While the PC is falling down; in the discharge (D) stage, the charged logic output node capacitor discharges, and the charge is flown back to the PC. In the final stage, the Idle (I) stage, when the PC is at its low, the output returns to its initial logic state. The operation is exemplified and demonstrated by the 2X1 MUX function shown in Fig. 1:

$$\boldsymbol{Y = A.S + B.\bar{S}}$$

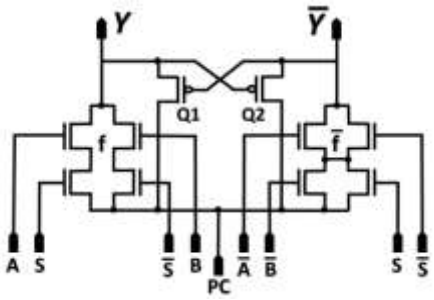

Figure 1. PTAL 2X1 Multiplexer

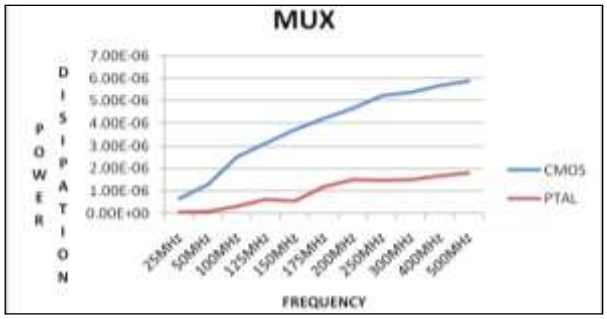

Figure 2. Power analysis for PTAL vs. CMOS 2x1 Mux

PTAL Mux comprises true complementary pass transistor NMOS functional blocks (F and $\bar{F}$), and a cross-coupled PMOS latch (Q1, Q2). In the beginning, PC = 0 and starts to ascend. Assume that the inputs A and S are both high and that a conducting path exists between the power-clock PC and the output Y. Given that f is connected to PC, Y will begin to rise from zero toward the PC's peak. The load capacitance of the successive gates will keep the node $\bar{Y}$ "tri-state" and near 0V.

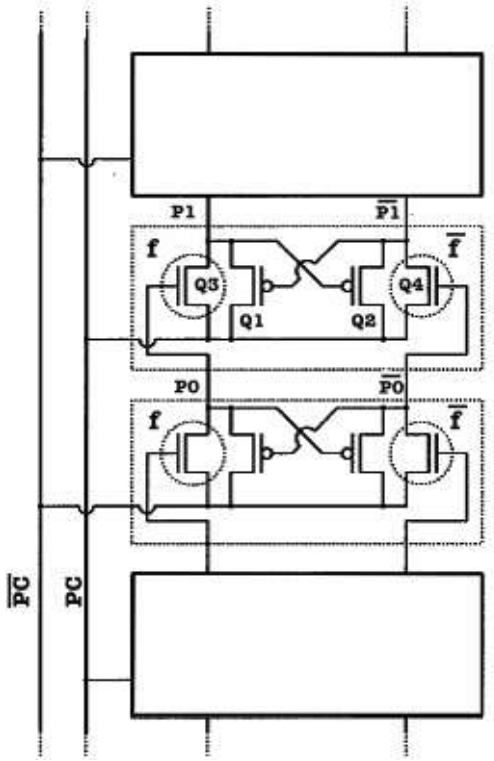

Figure 3. PTAL Shift Register

The PMOS Q1 with gate $\bar{Y}$ switches ON when the power clock PC ramps up, and the output Y is charged up to the peak of the PC. The gate Y of the PMOS Q2 will stay in the OFF state. After that, the power clock will ramp down to 0V, restoring the energy held in the Y output-node capacitance. The logic gate has a comparatively low level of complexity. Because of the PTAL's dual-rail design, the function also needs to be replicated as $\bar{Y}$. However, there may not always be 100% duplication because it is feasible to share transistors when creating NMOS functional blocks F and $\bar{F}$.

All Even-Logic stages in a sequence of PTAL gates are fed by the voltage-PC, but all Odd-Logic stages are fed by the inverted voltage-PC (phase-shifted by 180). PC and $\overline{PC}$ can both be produced by an effective single-inductor LC oscillator that serves as the PTAL power source. The stage-to-stage interface of the PC and $\overline{PC}$ with the series of PTAL logic gates is illustrated in Fig. 3, with a single NMOS pass transistor acting as the functional block per stage. A simple shift register exemplified in Fig. 3, is made up of a series of PTAL gates. Fig. 4 represents the schematic of PTAL-designed inverters in series. The power analysis simulation result shown in Figure 5, is obtained when a periodic binary sequence of '1010' is propagated through the series of PTAL inverters illustrated in Fig. 4. The energy consumption analysis demonstrates how energy is transferred from the power-clock supply to the output logic nodes and partly recovered back. When the PC is ascending, the output logic block is powered, and when it is falling, some energy is recovered. The simulation results claim that the energy loss in each clock period in this example is even less than 19 Fj/gate.

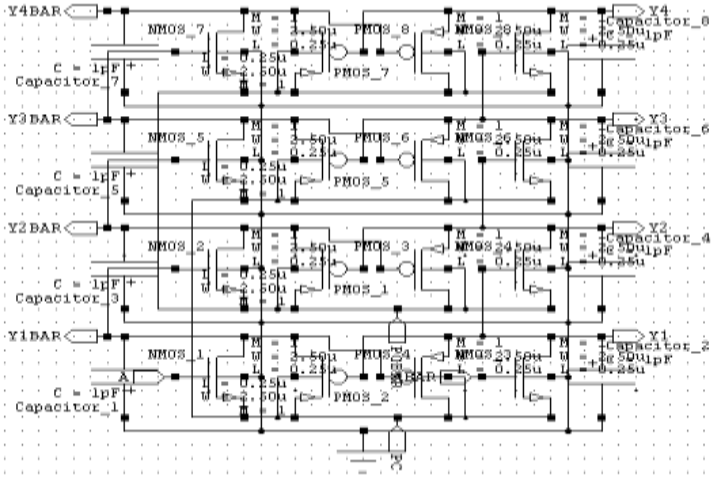

Figure 4. PTAL Inverter chain

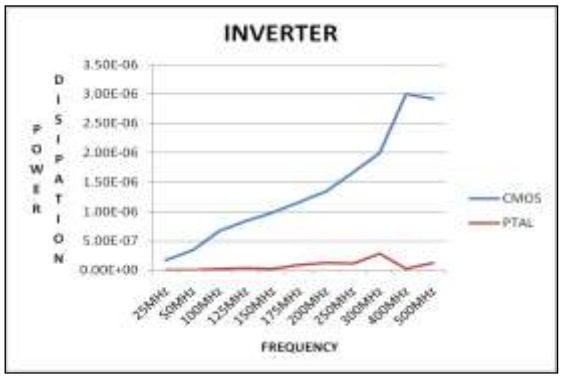

Figure 5. Power analysis for PTAL vs. CMOS inverter

The logic operation is divided into two primary phases: evaluate (E) while the power clock is climbing and discharge (D) when it is falling. The D phase of an even stage is the same as the E phase of an odd stage. When PC = 0, in Fig. 3, initially, both output nodes are discharged. When PC is ascending up, there is a path via one of the functional blocks during this E phase. The path exists because one of the logic inputs is at the power clock's maximum, which creates the route. The output node Y will consequently start to ramp up in sync with the power clock PC. When the output node capacitance reaches the peak of PC and the voltage between Y and $\bar{Y}$ exceeds Vtp (the PMOS threshold voltage), PMOS turns on. The PMOS device then transmits the charge to the output node (via the NMOS functional block F). The other PMOS device is kept in the OFF state throughout this clock

period because Y closely follows PC and is always greater than $\bar{Y}$. A tri-stated complimentary output $\bar{Y}$ should ideally remain at logic '0' while Y is following the power clock. The right logic levels may be sampled at the peak of the power clock, despite the tri-stated output being susceptible to parasitic charge coupling. The power clock descends down during the discharge phase. The PMOS device helps the output node discharge first. The logic high inputs are around PC's peak as PC gets closer to zero. The conducting functional block completes the last step of the discharge process. Both outputs may be drained to 0 volts using above-threshold logic low inputs without wasting energy.

4. PTAL Simulation Results

The schematic and the Spice simulation waveforms of various PTAL circuits were obtained by using standard 45nm technology with Vdd = 1V for various high-speed operating frequencies. The results of the designed PTAL circuits are compared for the performance and power dissipation with conventional CMOS logic under the same simulation conditions and inputs. It proves that even at high operating frequencies, it can outperform the dominating conventional CMOS logic design in the field of power dissipation. Simulation results for the basic logic gates and common digital circuits are compiled.

4.1 Two Input PTAL AND/NAND Gate

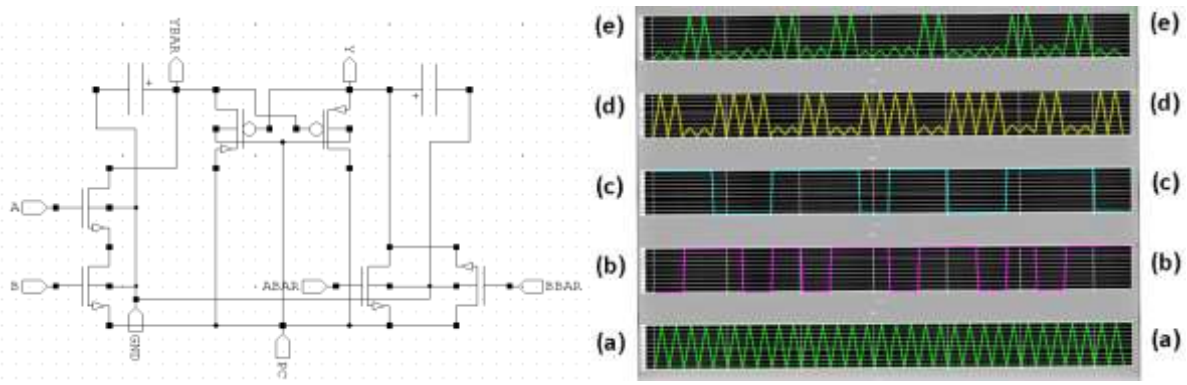

Figure 6. Schematic and Simulation Results of PTAL Two-Input AND / NAND Gate: (a) PC, (b) Input Signal A, (c) Input Signal B, (d) NAND Output (e) AND Output

The PTAL two-input NAND/ AND gate is implemented and simulated using standard 45nm technology. The schematic and the simulated waveforms are shown in Figure 6. The Power analysis of the circuit, PTAL vs. conventional CMOS logic is shown in Figure 7.

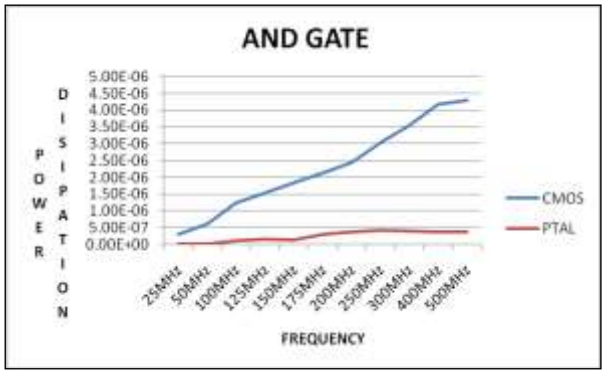

Figure 7. Power analysis for PTAL vs. CMOS AND gate

4.2 Two Input PTAL OR/NOR Gate

The PTAL two-input OR/NOR gate is implemented and simulated using standard 45nm technology. The schematic and the simulated waveforms are shown in Figure 8. The Power analysis of the circuit, PTAL vs. conventional CMOS is shown in Figure 9.

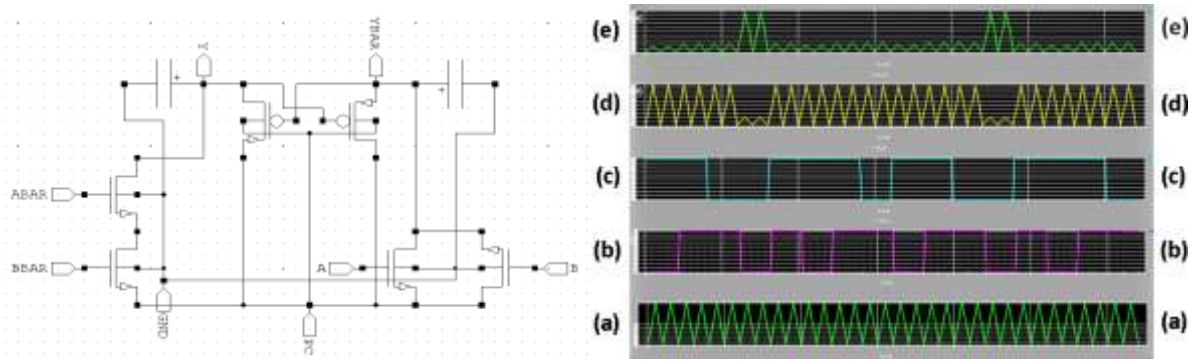

Figure 8. Schematic and Simulation Results of PTAL Two-Input OR / NOR Gate: (a) PC, (b) Input Signal A, (c) Input Signal B, (d) OR Output (e) NOR Output

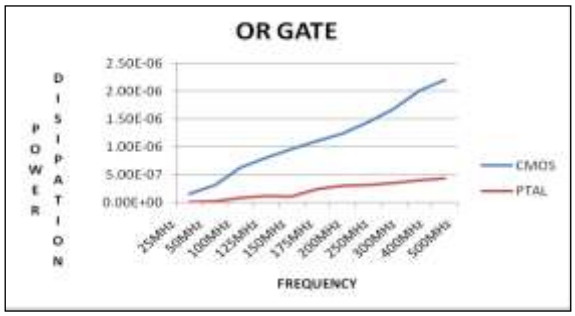

Figure 9. Power analysis for PTAL vs. CMOS OR gate

4.3 Two Input PTAL XOR/XNOR Gate

The PTAL two-input XOR/XNOR gate is implemented and simulated using standard 45nm technology. The schematic and the simulated waveforms are shown in Fig. 10. The Power analysis of the circuit, PTAL vs. conventional CMOS is shown in Figure 11.

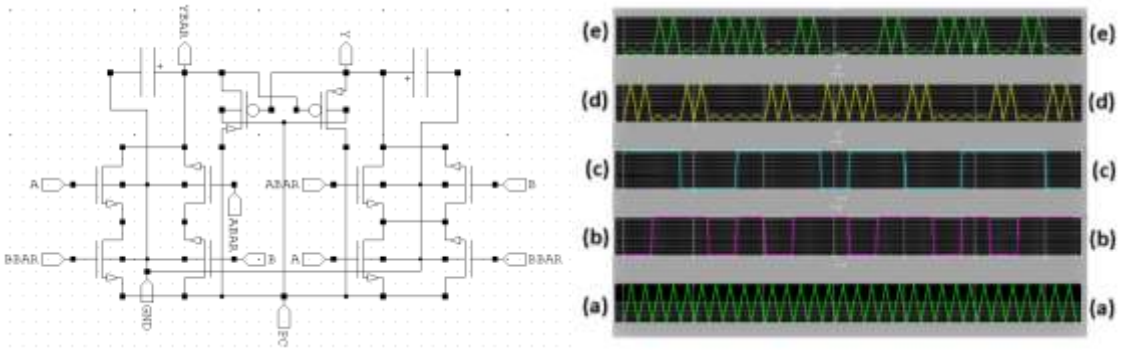

Figure 10. Schematic and Simulation Results of PTAL Two-Input XOR / XNOR Gate: (a) PC, (b) Input Signal A, (c) Input Signal B, (d) XOR Output, (e) XNOR Output

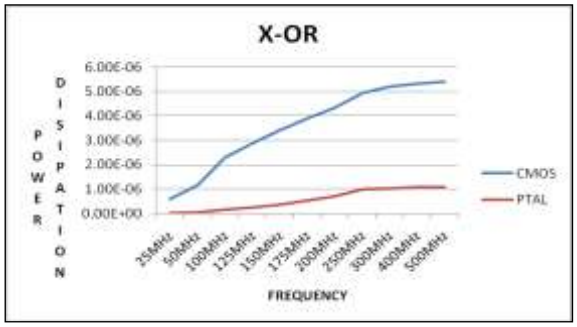

Figure 11. Power Analysis for PTAL vs. CMOS XOR gate

4.4 2x1 PTAL Multiplexer

The PTAL 2X1 Multiplexer is implemented and simulated using standard 45nm technology. The schematic and the simulated waveforms are shown in Fig. 12. The Power analysis of the circuit, PTAL vs. conventional CMOS is shown in Figure 13.

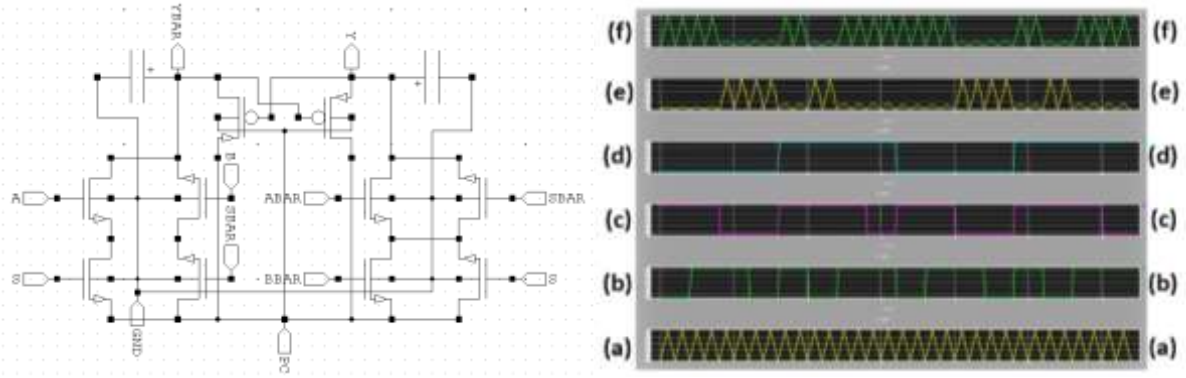

Figure 12. Schematic and Simulation Results of PTAL 2X1 MUX: (a) PC (b) Input Signal A (c) Input Signal B (d) Input Signal S (Select Bit) (e) MUX Output (f) $\overline{\text{MUX}}$ Output

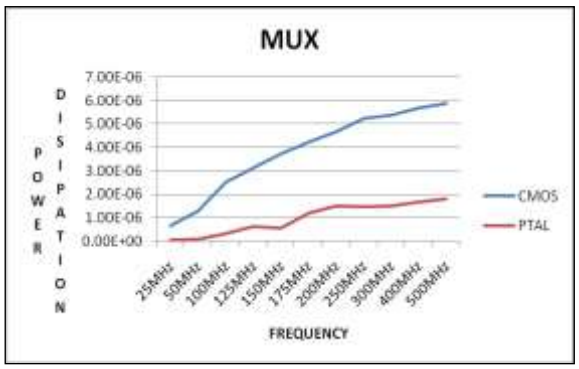

Figure 13. Power analysis for PTAL vs. CMOS MUX

5. Conclusions

We did a preliminary investigation of Fully Adiabatic Circuit Designing with Single Power Clock for High-Frequency Low-Power VLSI Circuits in this paper. Logically, we show that the proposed adiabatic circuit logic can save a significant amount of energy. Experiments on simple gates and more sophisticated arithmetic circuits backed up our theoretical findings. The fully Pass Transistor CMOS Adiabatic Logic (PTAL) circuit design was implemented and rigorously studied and analyzed against the conventional CMOS technology. We could conclude that PTAL supports dual-rail logic. It uses a single two-phase AC power clock to power both the rails. The complexity of proposed PTAL gate models is quite low as it consists of true and complementary NMOS functional blocks, as well as a pair of cross-coupled PMOS devices. The rigorous and precise simulation results claim that the modeled circuits can be operated even above 2 GHz clock frequency and power-clock supply down to 1V peak-to-peak using conventional 45nm technology. In terms of fast speed and energy consumption, it outperforms previously documented adiabatic logic approaches.

We pay a price for the power reductions we get from adiabatic circuits. We require specifically created charge recycling power-clock supply with lower related power dissipation. However, the use of charge in recycling power supply is essential for the successful implementation of adiabatic circuits in practice. Additionally, better circuit designs with fewer power-clock supplies must be developed along with fault tolerance, robustness, and resilience. These are a few of the areas that need further investigation and solid starting points for research and development in the stream of Fully Adiabatic Circuit Designing with Single Power Clock for High-Frequency Low-Power VLSI Circuits.

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