

The Hardware Design of Partial Discharge Online Monitoring for Large Power Transformers System

Zhen Guo, Yan Lu, Tianwei Zhang & Haijun Xin

School of Automaiton Engineering, QingDao Technological University

Tel: 86-532-8878-2001 E-mail: qs2004b@163.com

Abstract

The insulated state is one of the most important problems of large power transformer safely running in power system. The most efficient method in monitoring the running transformer's insulated state is to extract partial discharge (PD) signals in real-time. In this paper, a hardware system of partial discharge online monitoring for large power transformers is presented. In hardware circuit implementation, notice to choose signal sensors, A/D convert unit and filter circuit are reasonably designed, at the same time, large capability storage circuit and the fault diagnosis system are designed.

Keywords: Transformer, Partial discharge, Online monitoring

1. Instruction

Transformers are essential and important elements of electric power systems and their protections are critical,

The insulated state is one of the most important problems of large power transformer safely running in power system. The major cause of incipient faults is the deterioration of insulation in the transformers. When the condition of this equipment degenerates because of electrical, thermal, or chemical effects, intermittent incipient faults begin to persist in the equipment, till finally, a catastrophic failure occurs. Conventional protective devices cannot detect these incipient faults. Supplementary protective systems and methods, which may monitor the variable process of incipient faults online, are needed for power system transformers. Various incipient fault detection techniques, such as dissolved gas analysis and partial discharge analysis have been successfully applied to large power transformer fault diagnosis in past years. Since these techniques have high-cost and some are offline, a low-cost, online incipient fault detection for transformers would be very useful. Online condition monitoring of transformers can give early warning of electrical failure and could prevent catastrophic losses. Hence, in this paper, a powerful system based on digital signal processing is used in PD online monitoring for large power transformers. The paper gives an overview of the whole system, and its constituents are described in detail respectively.

2. System Composition

The basic structure of online PD monitoring system for large power transformers contains three parts: the current sensor system, the data sampling system based on DSP and the fault diagnosis system. The whole structure of this online monitoring system is as Fig. 1 shows. When PD phenomenon is generated in a transformer, current sensors will transmit the weak PD signals to the amplifier that magnifies the signals amplitude to meet the need of the A/D convert circuit. In the system, the antialiasing filter is used to limit the frequency pass band to decrease interferences. After A/D conversion, the analog signals are turned into digital signals, then the digital signals are stored temporarily in FIFO (First-In, First-Out) through further filtering process located in FPGA (Field Programmable Gate Array). Control circuit will arrange sequence between FIFO and DSP (Digital Signal Processor) for reading sampled data from FIFO to DSP.

3. The sensor system

Wideband current sensor and wideband amplifier make up the sensor system. The adopted current sensor is toroidal core and broadband active sensor with bandwidth from 10kHz to 1.2MHz, gain 5 or 10 times available. 12 current sensors will be installed on each of the transformers. The monitoring signals come from high-voltage, low-voltage bushings and ground wires of high-voltage, low-voltage side neutral point bushing terminal, transformer's shell, ground wire of core, and so on. Among them, transformer's shell and ground wires of high-voltage, low-voltage side neutral point bushing terminal are acted as main measurement points, the others as assistant measurement points. Depending on on-the-spot situation, two signals that come from main and assistant measurement point respectively are introduced to further process. The installation of these sensors does not change the transformer's original operation way. The structure of the sensor system is as Fig. 2 shows.

4. A/D converter unit

In this system, AD9224, a 12-bit, 40MSPS, analog-to-digital converter with an on-chip, high performance sample-and-hold amplifier and voltage reference is applied for transient nature and very short duration of PD signals. It

adopts a multistage differential pipelined architecture with output error correction logic to guarantee no missing codes over the full operation temperature range.

According to PD signals characteristic, a dc-coupled single-ended input mode would be appropriate for this data acquisition application, which strengthens the performance of anti-interference. At the same time, differential modes of operation provides the best THD (Total Harmonic Distortion) and SFDR (Spurious-Free Dynamic Range) performance over a wide frequency range. Differential operation requires that VINA and VINB of AD9224 be symmetrical driven, that is to say, the phase of two same inputs is in accordance after passing through the driven circuit. So, AD8056 plays the role of operational amplifier in the differential configuration. The internal structure of AD9224 is shown in Fig. 3 and the corresponding DC-Coupled differential input circuit is shown in Fig. 4.

5. DSP and FIFO interface and control circuit

In order to accelerate the transmission of the dataflow and overcome the problem of the bottleneck, an advanced modified Harvard architecture has been applied within VC5402 DSP. TMS320VC5402, a 16-bit high performance fixed-point digital signal processor of TI Company, is used for the main processor. This processor provides advanced multibus architecture, a 40-bit arithmetic logic unit (ALU) with a high degree of parallelism, on-chip memory, and additional on chip peripherals. Most of all, it has a highly specialized instruction set.

Because the sample rate of this system is up to dozens of MSPS (Mega samples per second), the data stored last time will be replaced by the following data soon if memory and control system cannot receive them in time, which is bound to cause the data confused. So, a high-speed buffer memory must be here in place. In this system, UPD42280, produced by NEC Company, is used to design the FIFO. Its capacity comes to 8-bit 256K (in fact 262224) bytes and it could complete per read and write within 30ns. Therefore, it is a kind of pretty ideal FIFO chip. With dynamic RAM structure in this chip, it can refresh itself automatically. It will go back to the first storing unit automatically after finished reading and writing the last storing unit. Fig. 5 illustrates the control circuit of FIFO and DSP.

Because AD9224 has 13 data lines (include OTR bit), it receives data by two FIFOs. In order to do this simultaneously by DSP control, the read pin /WE of two FIFOs must be connected with pin /Q of the JK trigger J1. Meantime, the /OE pin and the read reset /RES pin of two FIFOs are connected to the /Q pin of the JK trigger J2. Read clock of FIFO is offered by CLKOUT of the DSP.

On electricity, AD9224 begins the data conversion promptly with adding the clock signal. When writing data, the DSP makes Y0 low level through the decoding circuit. And the /WRST pin of two FIFOs turns into low level, then write address of FIFOs point to 0. Meanwhile, J1 is preset, which makes /WE pin output low level. Two FIFOs receive data that come from A/D circuit in synchronism from 0 address. Because there has no memory overwrite flag in FIFO and no start-stop sign in A/D, the DSP delays t (t is duration of FIFO converting from begin to end) through software. After the DSP writes 74LS138 /Y1 low level, a jump occurs in J1, the /WE pin turns on high level, writing operation is forbidden. When reading data, the /Y2 pin turns into low level under the DSP control. Then J2 is reset. The /Q pin outputs low level. The /RST pin and the /OE pin of the first FIFO are low level at the same time. Then read pointer locates in 0 address and allows the DSP to read the data through operation of the R/W pin and the /IOSTRB pin. After processing the data, the DSP writes decoder to make /Y3 low level again, then J2 jumps accordingly. The /Q pin outputs high level, so that the visit of first FIFO is forbidden. Meanwhile, the /Q pin rises to high level. So, it is allowed to read data of the second FIFO.

The clock input is referred to be an analog supply. A clock of high frequency is divided by frequency halving circuit to minimize the tolerance because AD9224 has a very tight clock tolerance at high frequency. The clock will provide clock signal to AD9224 and two FIFOs in the mean time. As being shown in Fig. 6. Because of time constrains of reading or writing in FIFO, the design sample clock fails to accomplish 40MHz. Therefore, the supreme clock of 33.3MHz has been adopted. The clock signal connects with CLK of A/D and WCK of FIFO respectively after frequency splitting by the 66.6MHz oscillator so that two FIFOs and AD9224 can use the same clock source to keep their time sequence strictly synchronized.

6. Fault diagnosis system

This data sampling system is mainly responsible for gathering PD signals of transformers and picking up PD characteristic parameters Φ -q-n online. Among them, Φ , q, n are the phase of PD signals, the discharge magnitude and the discharge repetitive rate, respectively. PD signals are continuously sampled by DSP in real-time with the high sampling rate and Φ , q, n are worked out to get Φ -q-n three-dimension fingerprint characteristic data. Then DSP transmits the discharge data to the fault diagnosis system according to standard communication protocol for further handling. The expert system of fault diagnosis judges the insulating condition of monitoring transformers and shows Φ -q-n three-dimension discharge fingerprint characteristic data

by many ways. The stored historical measurement data can be queried by staff members and remote management system. In normal operating state, the system can online monitor and write down the condition of transformers at any time, then analyze and judge the operation state of the equipment. When the transformer appears abnormally, the system should acquire, deal with the fault data rapidly, at the same time, it accomplishes the function of online calculation, store, statistic, warning, analyses report form, data transmission and so on.

7. Conclusion

In this paper, a hardware system of partial discharge online monitoring for large power transformers is presented which include signal sensors, A/D convert unit circuit and control circuit. The system automatically detect PD signals in large power transformers based on DSP. PD signals are obtained by the wideband current sensor that has enough anti-interference performance, sensitivity and linearity. The 16-bit high performance fixed-point TMS320VC5402 DSP is adopted as core processor, with its powerful and high-speed data processing ability, the system can accomplish complicated operation to sampled data and get the result promptly..

References

- A. Noro, K. Nakamura, T. Watanabe, and T. Morita. (1994). "Acoustic-based real-time partial discharge location in model transformers," in *Proc. Int. Conf. Signal Processing Applicat. Technol.*, 1994, pp. 1077-1082.
- Karen L. Butler-Purry and Mustafa Bagriyanik. (2003). "Characterization of transients in transformers using discrete wavelet transforms," *IEEE Trans. Power Systems*, vol. 18, pp. 648-656, May. 2003.
- M. A. Rahman and B. Jeyasurya. (1988). "A state-of-the-art review of transformer protection algorithms," *IEEE Trans. Power Delivery*, vol. 3, pp. 534-544, Apr. 1988.
- Ma Weiping, Dong Xuzhu, Wang Zhongdong, Zhu Deheng, Zheng Lianghua and Wang Shuo. (2000). "Research on on-line PD monitoring for large power transformers [J]." *CHINAPOWER*, vol. 4, pp. 35-37, 2000.
- Omar A. S. Youssef. (2003). "A wavelet-based technique for discrimination between faults and magnetizing inrush current in transformers," *IEEE Trans. Power Delivery*, vol. 18, pp.170-176, Jan. 2003.
- TMS320C54X DSP CPU and Peripherals Reference Set*, Volume 1, Texas Instruments, 2001.
- Xu Guizhi, Zhang Huifen and Sang Zaizhong. (2002). "Super-high speed A/D converter AD9224 and its applications." *International Electronic Elements*, vol. 4, pp. 48-50, Apr, 2002.

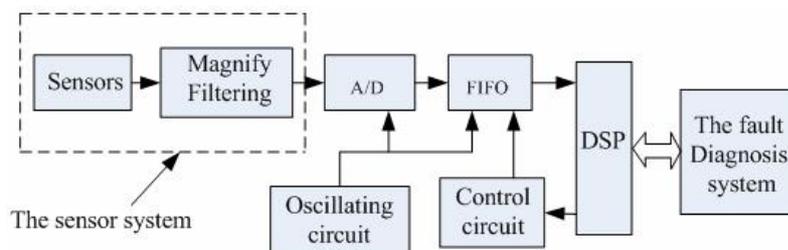


Figure 1. Block diagram of the system structure

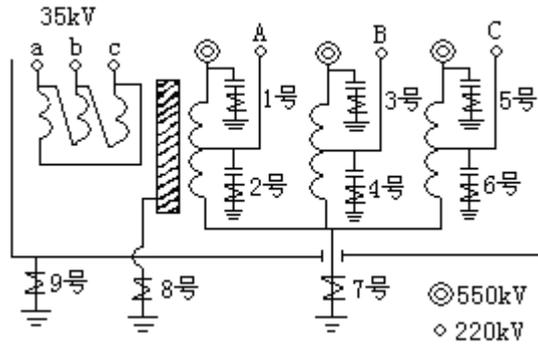


Figure 2. Install diagram of three phase winding transformer sensor system

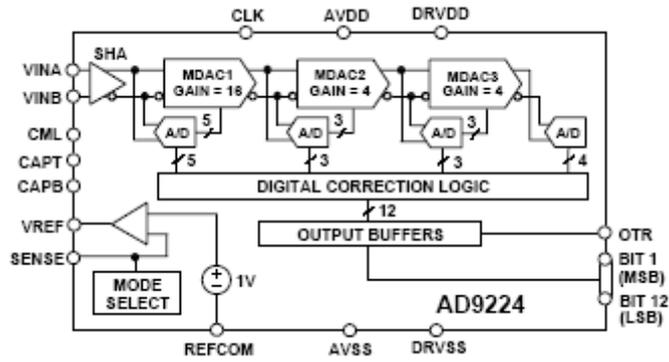


Figure 3. Internal structure of AD9224

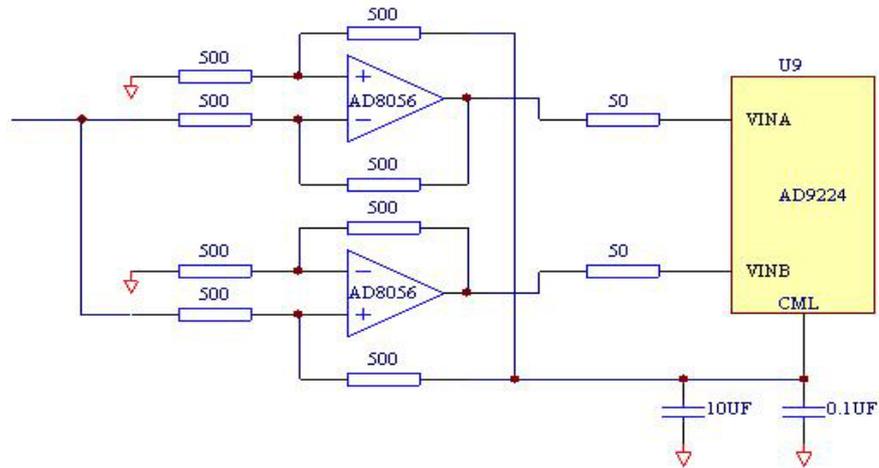


Figure 4. DC-Coupled differential input circuit

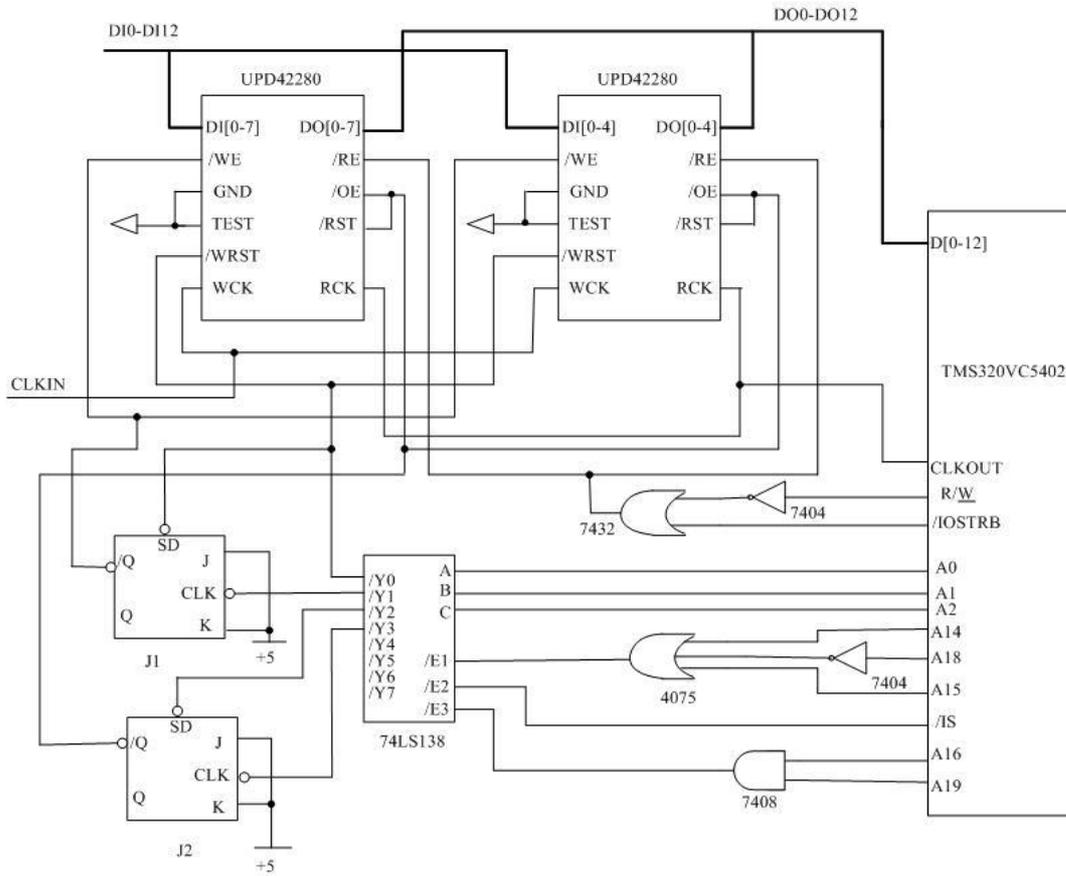


Figure 5. Control circuit of FIFO and DSP

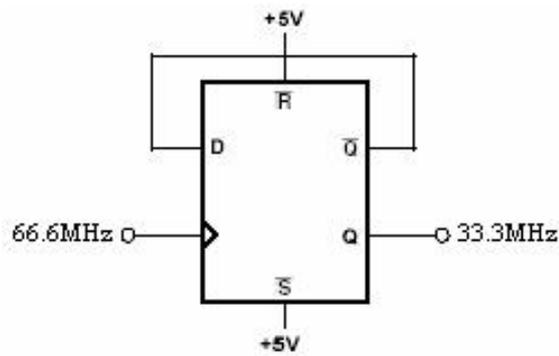


Figure 6. Divide-by two clock circuit