

A Low Drop-Out Voltage Regulator in 0.18 μm CMOS Technology

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Abstract

Low Dropout regulators (LDOs) are essential devices for power supplies in almost all portable and hand-held electronic devices. The chip area of the usual LDO is still large and does not have the flexibility or adjustability of sampling resistor, output resistor and capacitors in error amplifier and series pass element. In this study, a Low Dropout regulator (LDO) circuit architecture with Mentor Graphic simulation software in 0.18 μm CMOS process technology with adjustable sampling resistor, output resistor and capacitors in error amplifier and series pass element is proposed. The proposed regulator design has the superiority that the sampling resistor, output resistor and capacitor is adjustable or can be changed when needed in error amplifier and series pass element. Moreover, the occupied chip area obtained is only $(20.43 \times 14.6) \mu\text{m}^2$.

Keywords: Metal Oxide Semiconductor (CMOS), Low Dropout Regulators (LDOs)

1. Introduction

Low dropout regulators (LDOs) are widely used in power management integrated circuits and systems (Leung & Mok, 2003; Hazucha et al., 2004; Huang, Lu, & Liu, 2006; Uddin, Nordin, Reaz, & Bhuiyan, 2013). Such a regulator reduces the variations of voltage to a stable and acceptable level especially for product that are operated by portable battery such as cameras, hand phones, laptops. The study and research on power management techniques for different applications has been increasing rapidly for the last few years (Mohd-Yasin, Tan, & Reaz, 2004; Rosli, Mamun, Bhuiyan, & Husain, 2012; Chenchang & Hung, 2012; Peng, Changzhi, & Shuojie, 2012; Reaz et al., 2003; Nang, Ho, Jianping, & Or, 2011; Wu et al., 2011; Cheng, Yueh, & Liu, 2009; Akter, Reaz, Mohd-Yasin, & Choong, 2008) as a result of increased use of portable, handheld battery operated devices. Power management seeks to improve the power efficiency of devices resulting in prolonged battery life cycle and operating time for the device (Reaz, Choong, Sulaiman, & Mohd-Yasin, 2007; Akter, Reaz, Mohd-Yasin, & Choong, 2008; Romli, Mamun, Bhuiyan, & Hussain, 2012; Milliken, Martínez, & Sinencio, 2007; Kader, Rashid, Mamun, & Bhuiyan, 2012; Garimella & Furth, 2009; Marufuzzaman, Reaz, Rahman, & Ali, 2010; Arifin, Mamun, Bhuiyan, & Husain, 2012; Amin, Reaz, & Jalil, 2013; Reaz, Mohd-Yasin, Tan, Tan, & Ibrahimy, 2005).

There are several types of voltage regulators used in various electrical products such as Low Drop-Out (LDO) linear regulator, switching regulator, Switch-Capacitor Regulator (SCR) and each of these regulators has its own characteristics and applications (Reaz et al., 2003). The product that uses a low drop-out voltage regulator will give specified and stable voltages having low differences between its input and output voltages. The low dropout regulators have some good characteristics indeed, but they also have some problems in their implementations such as PSR and transient response etc. (Cheng, Yueh, & Liu, 2009). Regulating performances, quiescent current, operating voltages are the important characteristics to be considered during designing LDO. The other specifications are drop-out voltage, load regulation, line regulation, output voltage variation, output capacitor and ESR range and input/output voltage range (Ming, Li, Zhou, & Zhang, 2012; Majidzadeh, Schmid, & Leblebici, 2009; Guo, Shu, Zhang, & Zhao, 2007).

Basic LDO regulator topology usually consists of input voltage, reference, error amplifier, sampling resistor and series pass element that can be MOS-based or BJT-based as shown in Figure 1.

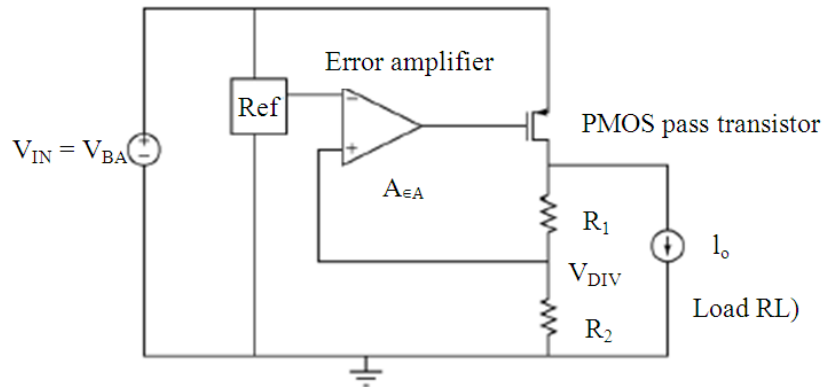


Figure 1. Basic LDO Topology

The operation of a low drop-out voltage regulator is based on feeding back an amplifier error signal to control the output current flow of the power transistor driving the load. The output voltage will be set to a stable voltage level by R_1 , R_2 and reference voltage. When there is change happen to output voltage, it will cause the divided voltage feedback through R_1 and R_2 and also include of reference voltage difference, it will force the error amplifier to adjust the current flow through PMOS. It will then provide a stable regulated voltage level. Output voltage can be determined by Equation 1 (Cheng, Yueh, & Liu, 2009):

$$V_o = V_{ref} \times (1 + R_1 / R_2) \quad (1)$$

Drop-out voltage is the minimum differential voltage between input and output where the circuit just stop to regulate. Usually drop-out voltage range for LDO regulator is from 0.1 to 1.5 V. The efficiency of LDO regulator can be calculated by using Equation 2 and drop-out voltage by using Equation 3 (Cheng, Yueh, & Liu, 2009):

$$\eta = \frac{V_{out}}{V_{in}} \quad (2)$$

$$V_{drop-out} = (1 - \eta) V_{in} \quad (3)$$

Therefore, in this study, a simple design of LDO regulator is proposed with slight modification from the usual design where there are provisions for adjustable components.

2. Materials and Methods

The objective of this study is to design and simulate a low drop-out voltage regulator for achieving a better output and making improvements compared to the circuit proposed by (Cheng, Yueh, & Liu, 2009). The software named Mentor Graphics by Emerald Systems is used for the design and simulation of the LDO. This software has two parts; first part is Design Architect IC (DA-IC) and second part is IC-Station. Design Architect has been used to design the schematics of the LDO regulator circuit and for the simulation to obtain the result. Then the IC-Station is used to design the layout of the schematic circuit.

The design of an LDO regulator circuit that contains an error amplifier, series pass element is shown in Figure 2 and the overall circuit that connect the error amplifier and series pass element with input voltage, reference voltage and sampling resistor shown in Figure 3. Error amplifier is used to scale down the output by comparing it against the reference voltage and also by adjusting the gate of series pass element to meet the requirement with the output voltage (Huang, Lu, & Liu, 2006). The series pass element is used to boost the output current capabilities of the error amplifier to the higher levels required by the load to maintain the constant output value. This involves transferring large currents from the source voltage to the load under low power supervision of the error amplifier. Sampling resistor is a feedback network that will scale down the output voltage to a suitable value to compare with reference voltage by the error amplifier. LDO regulator sometime requires off-chip external capacitor for stability and to improve the transient-response. Capacitor-free, low value and wide-range output capacitor features are becoming predominantly important for LDO regulator (Lin, Zheng, & Chen, 2008; Patel & Rincon-Mora, 2010).

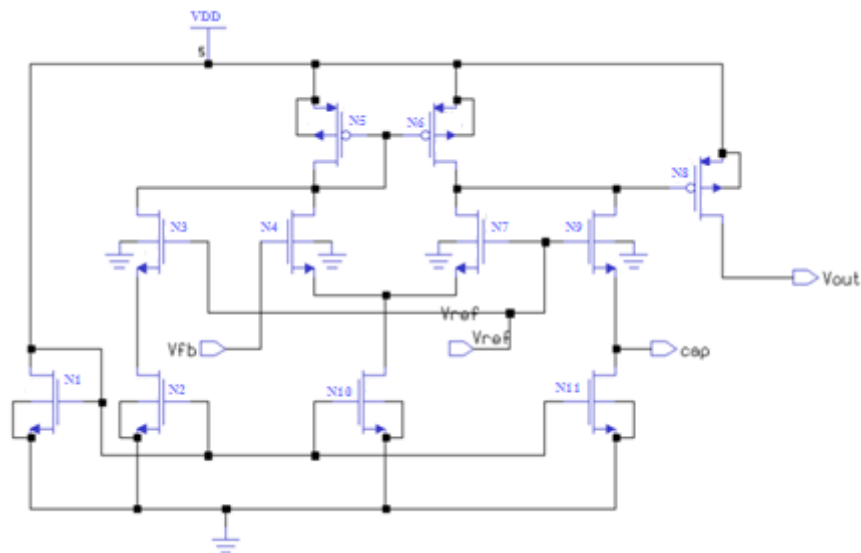


Figure 2. CMOS error amplifier and series pass element topology

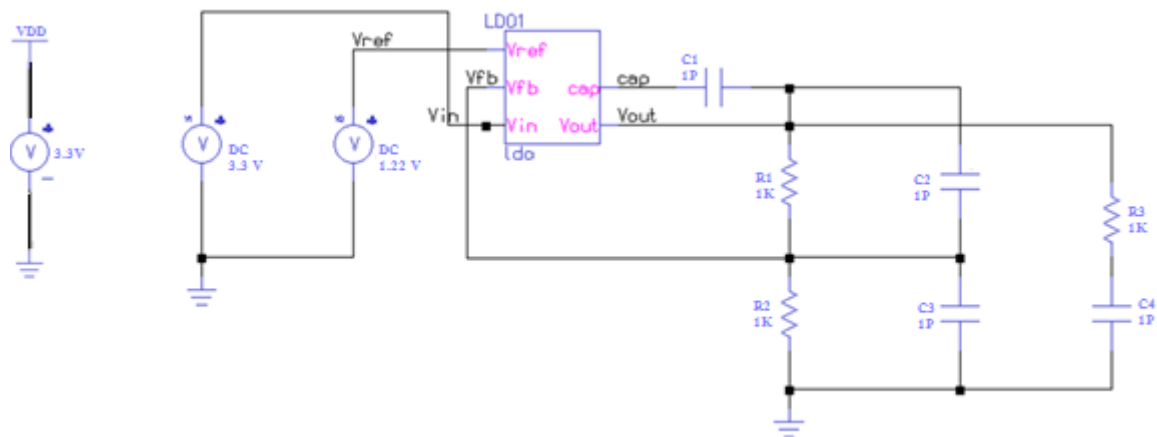


Figure 3. CMOS low drop-out topology

3. Results and Discussions

The LDO voltage regulator, implemented in 0.18 μm CMOS technology, with $V_{DD} = 3.3\text{ V}$, $V_{ref} = 1.22\text{ V}$ has been designed and simulated by Mentor graphics tool. Transient output variation is simulated by applying a transient load current signal and plotting the transient output voltage. The output voltage is 2.59 V as shown in Figure 4. Figure 5 shows the simulation of the loop gain and phase response of the proposed LDO regulator.

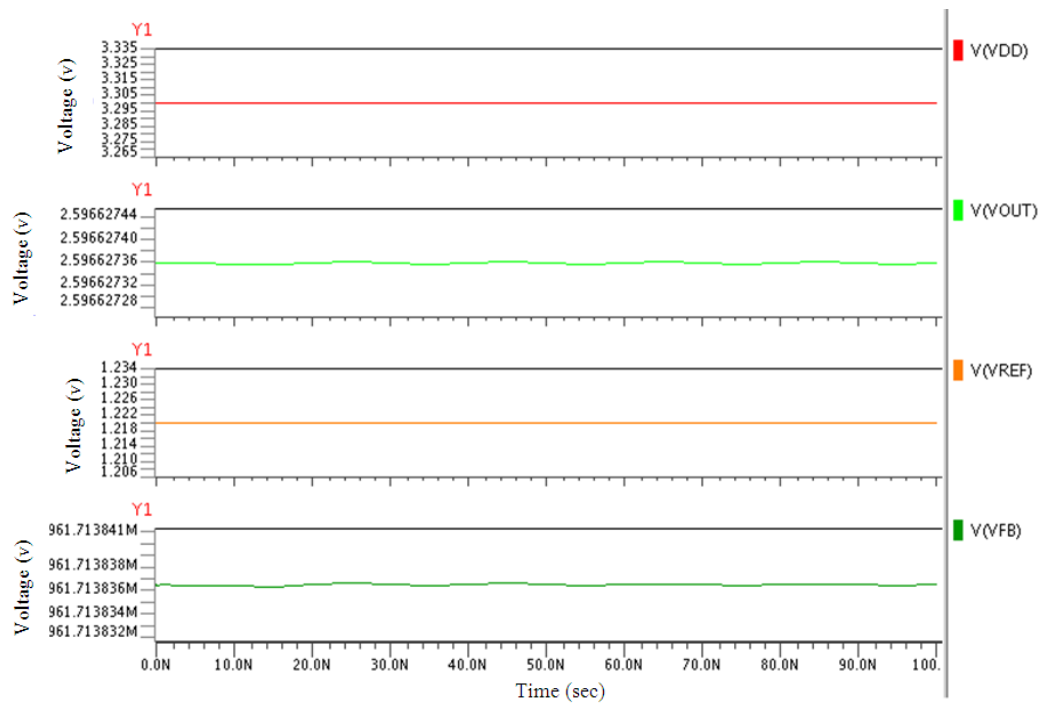


Figure 4. Transient regulation of low drop-out regulator

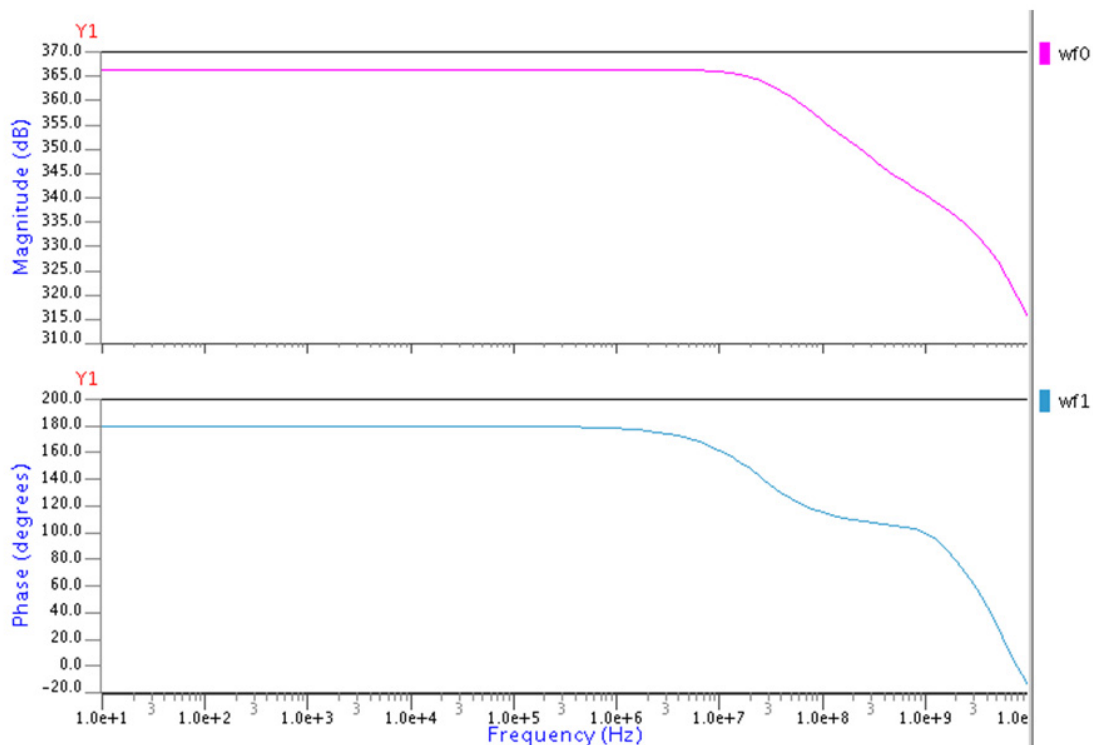


Figure 5. Loop gain and phase response of the purpose LDO

Figure 6 shows the CMOS layout of the LDO regulator. The layout has been done by using Mentor Graphics IC-Station in 0.18 μm CMOS technology. The layout of LDO regulator occupies $(20.43 \times 14.6) \mu\text{m}^2$ of silicon area. This layout just include error amplifier and series pass element. The input voltage, reference voltage, sampling resistor and load will be connected to this layout through in input and output.

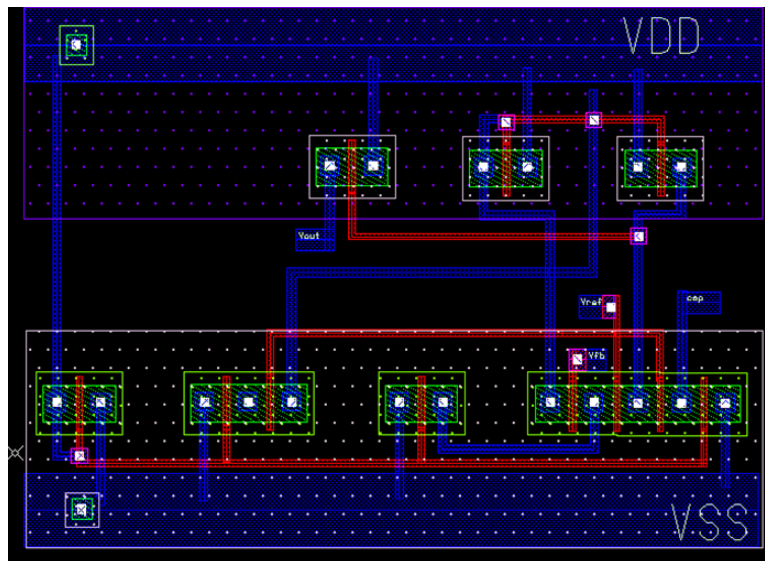


Figure 6. CMOS low drop-out layout

4. Conclusion

Low drop-out regulators are essential for many portable devices including camera, laptop, hand-phone etc. LDO regulator can supply a constant output voltage and also can yield less noise than switching regulator although LDO power efficiency is usually less than switching regulator. The proposed regulator design has the superiority that the sampling resistor, output resistor and capacitor can be adjustable or can be changed when needed in error amplifier and series pass element.

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