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Presenting Systematic Design for UWB Low Noise Amplifier Circuits

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Abstract

A systematic approach to CMOS Low Noise Amplifier design is presented. This approach uses an input impedance matching technique based on LC Ladder filters which will provide suitable input matching in any arbitrary band (S11<-10dB), also S22 is about -10 dB in average. Using cascode structure, maximum power gain about 25 dB is achievable. Noise level is less than 3 dB over the full band of UWB. Power dissipation of this amplifier is only 8.5 mw and operates with 0.85 v supply voltage while 0.13 μm CMOS technology is used.

Keywords: LNA, ultra-wideband, impedance matching, inductive degeneration, NF

1. Introduction

Low noise amplifier is the most important component of the receiver, due to the fact that it can determine the total noise level of the receiver system. Designing this part includes many constraints which make total design challenging. Some of these considerations are low noise level, sufficient gain without contributing much noise, input and output matching improvement and low power consumption. Also telecommunication technology improvement and increasing data transferring rate, require new designs working in wide and high frequency bands which make design more complicated. So it seems that designing a systematic approach which comply all of these considerations in wide and high arbitrary band of frequency is useful.

One of the major applications of wide frequency bands is Ultra-Wideband (UWB). It may be used to refer to any radio technology having bandwidth exceeding the lesser of 500 MHz or 20% of the arithmetic center frequency, according to Federal Communications Commission (FCC). This band was first used by military of America but because of attractive advantages and technology improvement, FCC authorized the unlicensed use of UWB in 3.1-10.6 GHz.

The purpose of this paper is presenting a systematic design for LNAs which are used in any frequency bands of ultra wide band, based on mathematical relations.

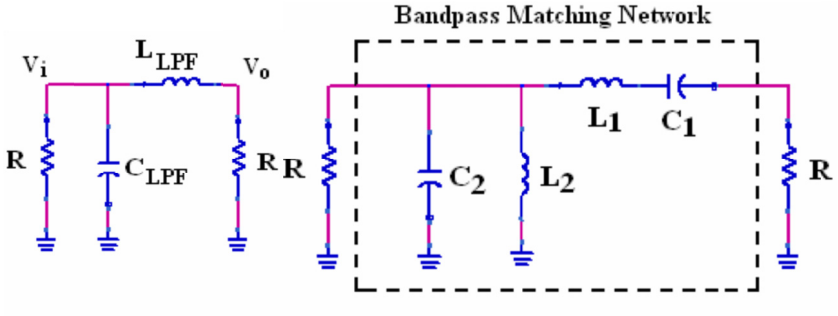
Any low noise amplifier has three parts which must be designed carefully. The first and important part of LNA is input impedance matching. Design theory and the relevant equations for input matching are given in section (2). Second is designing the transistor core of the amplifier for amplifying received signal, this part is designed in section (3) and (4). After input impedance matching and amplifier designing, output impedance matching has an important role in LNA design. This part is considered in section (5). At the end the accuracy of this method will be shown by simulation results for 2 selected bands in section (6).

2. Input Impedance Matching

Input and output of LNA must possess a stable input and output impedance for about 50 Ω over the frequency range of interest. There are a lot of ways for input impedance matching. One of the simplest methods is using simple resistor, but as you know thermal noise of resistor will increase noise level and power dissipation directly. Using shunt feedback resistor is another way of input matching which could reach good noise performance and suitable gain with using multi stages. One of the most attractive methods is inductive degeneration which was first introduced for narrow band amplifiers. Using band pass filter instead of low pass will increase band width of this method, which our design approach is based on this point (Lee et al., 2005). Proper design could provide

a constant 50 Ω resistor at the input of the amplifier. This method has low noise level because of using noise less components like inductors and capacitances.

Designing good band pass filter is based on designing good low pass one. Our selected low pass filter is shown in Figure 1(a).



(a) (b)

Figure 1. (a) Low pass filter (b) Band Pass Filter derived from low pass filter

First we must calculate transformation function and the value of low pass filter, after simplifying we will reach Equation (1) and Equation (2).

$$H(j\omega)=\frac{Vo}{Vi}=\frac{2-\omega^2LC}{(2-\omega^2LC)^2+(\omega L/R+\omega C)^2}+j\frac{-(\omega L/R+R\omega C)}{(2-\omega^2LC)^2+(\omega L/R+\omega C)^2} \tag{1}$$

$$|H(j\omega)|=\frac{(2-\omega^2LC)^2+(\omega L/R+\omega C)^2}{\left\{(2-\omega^2LC)^2+(\omega L/R+\omega C)^2\right\}^2} \tag{2}$$

At which $L=L_{LPF}$ and $C=C_{LPF}$.

The value of $|H(j\omega)|$ in cut off frequency is obvious from the circuit and it is equal to $1/2\sqrt{2}$. So from Eq. (2), we will have:

$$\left\{(2-\omega_c{}^2LC)^2+(\omega_cL/R+\omega_cC)^2\right\}^2=8 \tag{3}$$

This equation has a lot of results which just one of them has response and it is coming below:

$$\begin{cases}(2-\omega_c{}^2LC)^2=0\\(\omega_cL/R+\omega_cC)^2=8\end{cases} \tag{4}$$

By simplifying this equation the values of inductor and capacitor in low pass filter could be found.

$$L_{LPF}=\frac{\sqrt{2}R}{\omega_c},\quad C_{LPF}=\frac{\sqrt{2}}{R\omega_c} \tag{5}$$

According to Figure 1(b) and using low pass to band pass transformation formulas (Lee et al., 2005), the values for band pass filter components will be found.

$$r=\frac{\omega_c}{BW}\rightarrow L_1=rL_{LPF},\quad C_2=rC_{LPF},\quad C_1=\frac{1}{\omega_c{}^2L_1},\quad L_2=\frac{1}{\omega_c{}^2C_2} \tag{6}$$

BW is an abbreviation of the Bandwidth and ω_c is the central frequency of the band of interest which could be

determined by $BW = \omega_H - \omega_L$ and $\omega_c = \omega_L + \frac{\omega_H - \omega_L}{2}$, ω_L and ω_H are the low and high stop frequencies respectively.

3. LNA Structure and Transistors Size

In order to isolate input and output of the amplifier and providing suitable gain, without occupying a lot of space on the chip, we choose cascode structure for the core of the amplifier. As it is shown in Figure 2, the band pass filter must be stuck to the cascode stage. So gate-source capacitance of first transistor could have the same function as C_1 in band pass filter. Now we must choose the size of transistors. As we define C_1 equal to C_{gs}, by using C_{gs} formula the width of transistor will be found (Razavi, 1998).

$$Cgs = \frac{2}{3} CoxWL \rightarrow W = \frac{3}{2}\frac{Cgs}{CoxL} \tag{7}$$

For take of simplicity, the size of transistors in cascode structure must be equal.

4. Evaluating Ls, Lg and Biasing Voltages

According to Figure 2, the input impedance of the first transistor (M1) must be calculated. It is shown in Equation (8).

$$Z = R + jX = \frac{g_m L_s}{C_{gs}} + j(\omega L_s - \frac{1}{\omega C_{gs}}) \tag{8}$$

It is clear that imaginary part of input impedance must be zero in resonance frequency but real part of it must be equal to 50 Ω.

Simplifying real part of this impedance and paying attention to $gm = \mu_n C_{ox} (W/L) V_{eff}$ and $Cgs = \frac{2}{3}(C_{ox} WL)$ formulas, we could find good values for Ls and V_{eff} (which effective voltage is Vgs-V_{th0}).

$$R = \frac{3\mu_n V_{eff} L_s}{2L^2} \rightarrow V_{eff} L_s = \frac{2RL^2}{3\mu_n} \tag{9}$$

Choosing low values for Ls will increase effective voltage which directly increases biasing voltages and power consumption. By choosing a good value for L_s, V_{eff} will be identified. Since L_1 in band pass filter is equal to L_s+L_g in Figure 2 and it must resonance with C_{gs} in resonance frequency, L_g value will be found.

Considering MOSFET saturation condition ($Vgs > |Vth0|$ and $Vgd < |Vth0|$) V_{bias1} and V_{bias2} and V_{dd} will recognize.

5. Output Impedance Matching

A simple way for output matching is using source follower stage (Roodaki et al., 2008). Output impedance of this stage is simply defined by $1/g_{ms}$ where g_{ms} a gate-source trans-conductance of the source follower. According to value of g_{ms} and current formulas, current bias will choose simply.

Figure 2 shows the overall schematic of LNA. We assume L_{RFC} equal to 2nH.

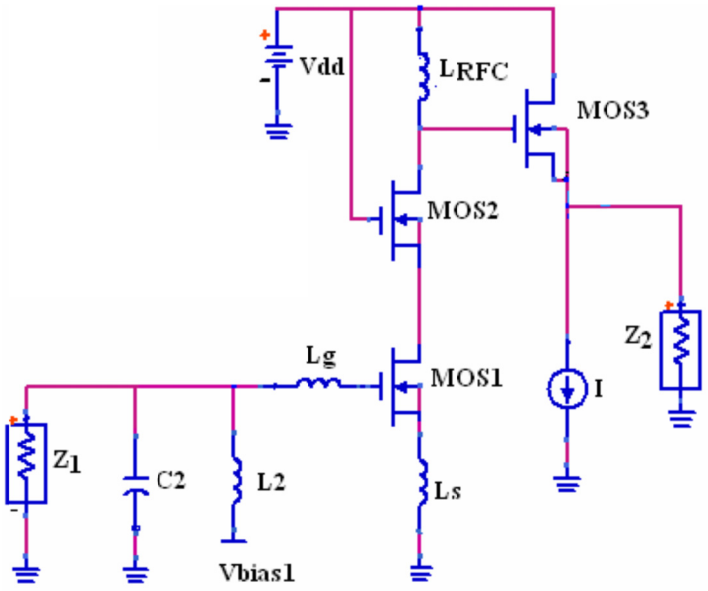
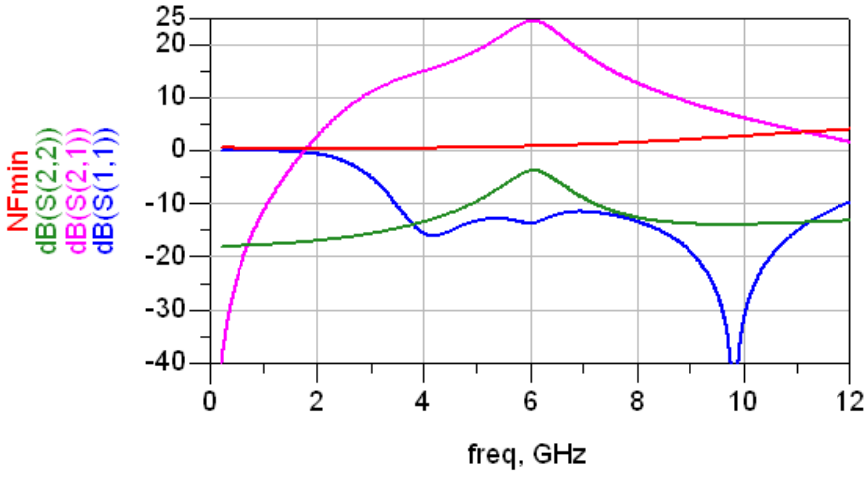


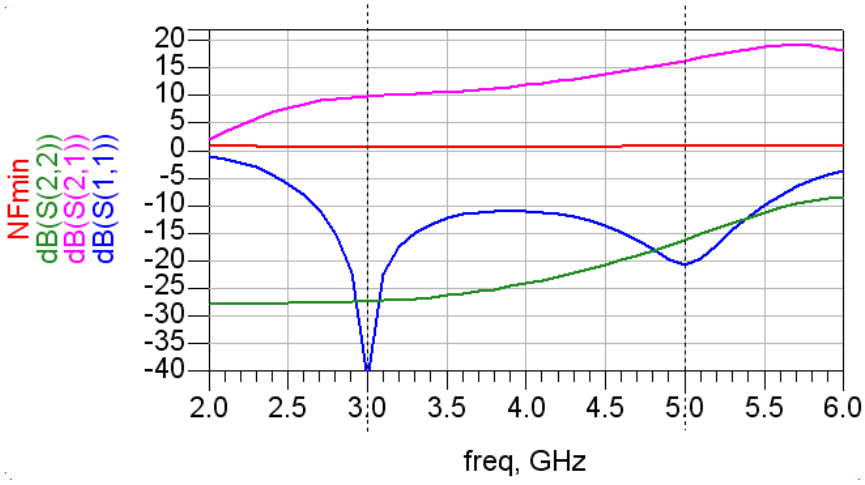
Figure 2. Overall schematic of designed LNA

6. Simulation Results

Simulation Results for full band of UWB are shown in Figure 3(a). S11 which shows input impedance matching is below -12 B all over the full band and shows the accuracy of mathematical analysis. S22 is about -10 B in average over the target bandwidth which they show reasonable input and output matching for a systematic approach design. S21 which shows the overall gain is as high 25 B in middle frequency. The LNA simulation gives a low noise level less than 2 B because of using noise less components on this architecture. Since we use cascode architecture S12 is less than -50 B and shows good isolating between input and output of LNA.



(a)



(b)

Figure 3. Simulation Results

Since we addressed this method as a systematic approach, it must operate in all arbitrary bands. For testing this approach in other bands one of the most usage bands in UWB was selected. 3-5 GHz simulation results are shown in Figure 3(b). As you see S11 is again less than -10 dB and S22 is les than -15 dB. Noise level of LNA in this band is less than 0.8 dB and shows very good noise performance. S21 is about 12 dB in average.

7. Conclusion

Based on the theoretical and mathematical analysis, a systematic procedure for design of UWB CMOS LNA was presented. The designed LNA for arbitrary band of frequency achieves up to maximum 10 dB power gain with a suppressed NF less than 2 dB and provides good input and output matching less than -10 dB. The designed LNA consumes only 8.5 mw with 0.85 *v* supply voltage.

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