Systematic Approach for Designing Ultra Wide Band Power Amplifier

Yadollah Rezazadeh[1], Parviz Amiri[1] & Maryam Baghban Kondori[2]

[1] Electrical and Computer engineering Department, Shahid Rajaee Teacher Training University, Iran

[2] Space Research Institute (SRI) of Iranian Space Agency (ISA), Tehran, Iran

Correspondence: Yadollah Rezazadeh, Electrical and Computer engineering Department, Shahid Rajaee Teacher Training University, Lavizan, Babaee Highway, Tehran, Iran. E-mail: rezazadeh@srttu.edu

Abstract

In this work a systematic approach is presented for an allover design of full band UWB power amplifier. Purposed approach is included in three main steps, which are CMOS amplifier core stage bias design, input matching network and output matching network design, respectively. The first step starts by considering a cascode stage which can obtain power consumption and gain conditions through mentioned equations. Second and third stages are done through designing wide band LC networks for obtaining bandwidth requirements of UWB. For show performance of presented approach, we have designed a UWB PA through these steps. Simulation results show the performance of this design procedure.

Keywords: UWB, impedance matching, RFC

1. Introduction

Wireless communications are very important nowadays, because they can give portability to electronic devices and can also eliminate wires from systems while providing fast speed to data transmission. Designing wideband, efficient and low consumption systems for these purposes are still a challenge for electronics engineers. One of the technologies which provide great specifications for some kind of data transmission techniques like OFDM and CDMA in required bandwidth and data rate of short distance communication is ultra-wideband technology approved for unlicensed use in 2002 by FCC (Liu R. C., Deng K. L., & Wang H., 2003). This technology works in wide band frequency of 3.1 GHz to 10.6 GHz.

Transceivers should be designed for operating in this wide band. Power amplifiers (PA) are the most important front end of the transmitter systems which can boost the signal power to the certain level allowed by FCC rule. Output signal power should not exceed -41.3 dBm/MHz it means that power delivered to the load in UWB PA must be lower than 1.2 mW. On the other hand we have to consider matching for input and output of this amplifier because any mismatch can cause signal power loss and fail in amplifying and transmitting signal. In this step we mainly use passive LC elements for matching networks because their power consumption is very low and negligible. Purposed design procedure is applicable for other kinds of PAs. Purposed procedure can result in an ultimate low voltage and relatively high efficiency circuit in comparison with already purposed PAs (Wang R. L., Su Y. K., & Liu C. H., 2006; Lu C., Pham A., & Shaw M. 2006; Hsu H. C., Wang Z. W., & Ma G. K., 2005).

2. CMOS Amplifier Stage Design

The main part of the PA is the transistor stage of it because we can define the bias conditions so that amplifier operates in desired class. Efficiency and linearity of the circuit depends on class of operation. We try to set a bias for obtaining class AB which can provide good efficiency and linearity to the system.
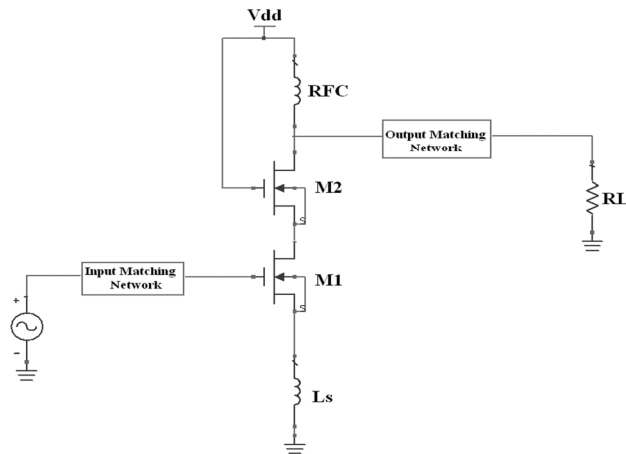
Figure 1. General structure of the PA

First of all we have to know how much power is needed to be delivered to 50 ohms load (next stage), so we can calculate the value of resistance that 50 ohms load should be transferred to in the drain of M2, through the impedance matching network at output using Eq. (1).We should assume a voltage supply value for this part (for example 1.2 v in our work).

$$P_l = \frac{V^2}{R_L} \tag{1}$$

Afterwards we need to find appropriate drain current and gate source voltage which is suitable for setting MOSFETS working in class AB. These values can be achieved referring to the Id-Vds and Id-Vgs characteristics of the applied MOSFETs. We will use 0.18 um CMOS technology in section 5. Right now we are ready to calculate W/L of the cascode stages through drain current equation, Eq. (2), while we choose 0.2 v for overdrive voltage (Razavi B., 2000).

$$I_d = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})(V_{GS} - V_{TH})^2 \tag{2}$$

We can calculate the voltage gain of the amplifier through Eq. (3) to (7) where Ro, cascade, gm, ro, RL, λ stand for equivalent output resistance of cascode stage, transconductance of the MOSFETs, drain source resistance of the MOSFETs and channel length modulation coefficient of the MOSFETs in Figure 1, respectively. We can increase total gain of the amplifier by increasing L and W so that the (W/L) remains constant, because $\lambda \propto 1/L$ so it will increase gm and consequently the gain.

$$R_{o,cascode} = gm_2 ro1 ro2 \tag{3}$$

$$gain_{cascode} = gm1((gm2 ro1 ro2) || R_L) \tag{4}$$

$$gm = \sqrt{2\mu_n C_{ox}(\frac{W}{L})I_d} \tag{5}$$

$$gm1 \approx gm2 = gm \tag{6}$$

$$ro1 = ro2 = \frac{1}{\lambda I_d} \qquad\qquad I_{d1} = I_{d2} = I_d \tag{7}$$

3. UWB Input Matching Network Design

One of the most important considerations in designing high frequency amplifiers is impedance matching or impedance transferring which is performed for transferring an impedance value to the desirable value. This helps maximum power transmission and consequently obtaining maximum power gain.

For low consumption reason, we have to design matching circuits by reactive and lossless elements. Here we use LC ladder network for impedance matching. General structure of this network and its sub-networks are shown in Figure 2 in which Rs, Rp and jXs/pn is stand for output impedance of source, input impedance of the next stage

and impedance value of a reactive element (capacitor or inductor), respectively.
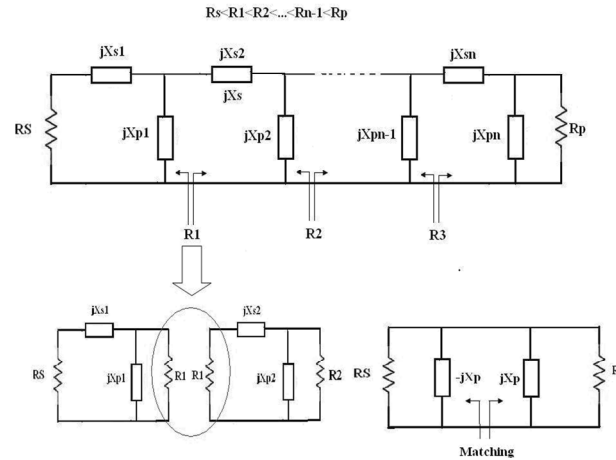
Figure 2. Ladder matching network, one of the sub-networks and matching equivalent for L sub-circuit

We can derive some equations for calculating the value of each Xs/pn. After calculating absolute value for each of them we can replace a capacitor or inductor according to the application of each element. Because of integrated circuit considerations on minimum area occupying, we have to use inductors and capacitors as less as possible, so usually we try to obtain matching requirements by only a two stage ladder network and we provide related equations.

As it's shown in Figure 2, Ladder network is constructed from sub-circuits named L networks; also the matching equivalent of an L network is shown.

If we have a series combination of a resistor Rs and reactance Xs, equivalent impedance Zs and quality factor Qs can be calculated through Eq. 9.

$$Zs = Rs + jXs \,, \quad Qs = \frac{|Xs|}{Rs} \tag{9}$$

The same parameters can be derived for parallel combination of Xp and Rp through Eq. 10.

$$Zp = \frac{jRpXp}{Rp + jXp} \,, \quad Qp = \frac{Rp}{|Xp|} \tag{10}$$

If we want to obtain an equivalent parallel circuit from series or vice versa, we have to apply Eq. 11 and 12 for calculating new values

$$Rs = \frac{Rp}{1 + Qp^2} \,, \quad Xs = \frac{Qp^2}{1 + Qp^2} Xp \tag{11}$$

$$Rp = (1 + Qp^2)Rs \,, \quad Xp = \frac{1 + Qp^2}{Qp^2} Xs \tag{12}$$

According to definition of the Qs, and set it equal to Qp, we have Eq. 13.

$$Qs = \frac{|Xs|}{Rs} = Qp \tag{13}$$

For the first sub-circuit in Figure 2 we assume that R1>Rs and Xp1Xs1<0. matching will be occurred if Rs transformed to R1 and Xs1 to -Xp1 (to have conjucated impedances in both sides) Eq. 11-13 implies Eq. 14 for obtaining conjucation condition

$$Qs = Qp = \sqrt{\frac{R1}{Rs} - 1} \tag{14}$$

So we can calculate reactance values through Eq. 15.

$$|Xs1| = RsQs1 \,, \quad |Xp1| = \frac{R1}{Qp1} \tag{15}$$

This single stage is able to do the complete matching just in one frequency and the bandwidth is B=f0/Qt in which Qt is the total quality factor of the circuit.

$$Qt = \frac{Rp \, / \, 2}{|Xp|} = \frac{1}{2}Qp = \frac{1}{2}Qs \tag{16}$$

Right now we can generalize this procedure to more stages and obtain desirable wider bandwidth. For this object we assume R1 as a virtual resistance and couple it to the next L stage this is illustrated in Figure 2. Related values for two stage ladder is calculated simply by equating quality factor of two consequent L networks and finally results Eq. 17.

$$\frac{R1}{RS} = \frac{R2}{R1} \,, Q = \sqrt{\frac{R1}{Rs} - 1}$$

$$|XS1| = Q \times RS \,, \quad |XS2| = Q \times R1 \tag{17}$$

$$|XP1| = \frac{R2}{Q} \,, \quad |XP2| = \frac{RS}{Q}$$

Applying capacitor and inductor definition we can find their related values (Eq. 18).
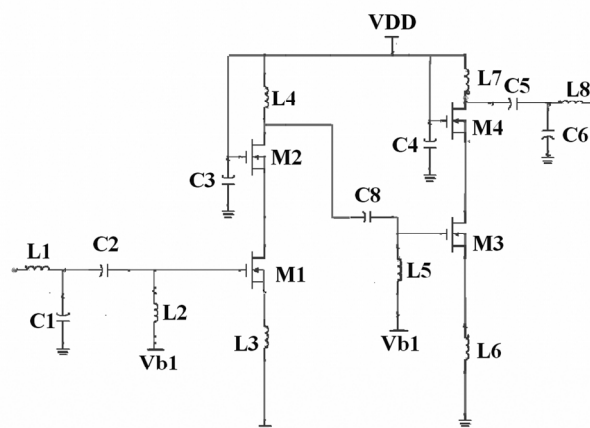
$$L1 = \frac{XS1}{2\pi f_0} \,, \quad L2 = \frac{XP2}{2\pi f_0} \,, \quad C1 = \frac{1}{2\pi f_0 XP1} \,, \quad C2 = \frac{1}{2\pi f_0 XS2} \tag{18}$$

4. Output Matching Network Design

It's possible to design Output matching circuit through the same procedure done for the input matching. In this circuit the RFC and dc canceller capacitor will be a part of ladder network we have to add another capacitor and inductor as the next stage of the matching network. This output matching circuit will be terminated by a 50 ohms resistive load. We have to set the network so that output transistor see a resistance equal to RL in the output because of above explained reasons. By all means matching network should transform 50 ohms load impedance to RL connected to the output transistor drain.

5. A UWB PA through the Purposed Design Procedure

In this part we have purposed a full band UWB PA. Figure 3(a). Figure 3 illustrates the circuit schematic of this PA. Simulation results show that the power dissipation is 25.25 mW. S-parameters diagrams are shown in Figure 3(b).

(a)

(b)
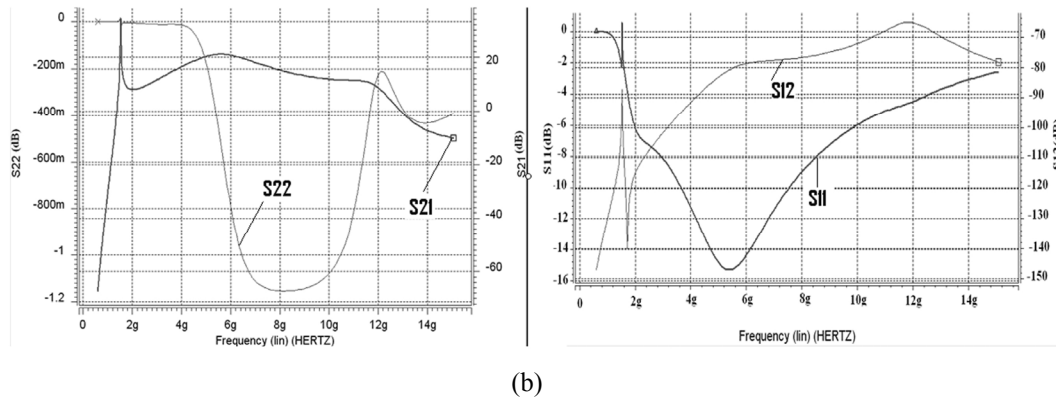
Figure 3. (a) Circuit schematic of the UWB PA (b) S-parameter simulation results: left diagrams - S22 and right axis is belonging to it. S21 is related to left vertical axis. Right diagrams - S11 and right vertical axis is belonging to it. S12 is related to left vertical axis

6. Conclusion

A design procedure purposed for UWB PA. Cascode structure was used for amplifier stage because of its unique property in increasing bandwidth and gain. Overall Biasing procedure explained including related equations needed for designing each element. We used ladder LC network for input and output matching network. Equations provided for calculating each element. Finally a UWB PA was designed through this procedure and simulation results for s-parameters shown in Figure 3(b). Simulation result shows total power dissipation is 25.25 mW.

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