Used in Image Acquisition Area CCD Driving Circuit Design

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Abstract

To satisfy the demands such as high integrated degree and the handling of real time of the area CCD image collection system, according to the structural characteristic of area CCD, this paper has designed a kind of high integrated degree drive circuit. Through analyzing the internal structure and the characteristic of driving signals of area CCD, the driving circuit of area CCD have gone on suit and simplify, at the same time, FPGA that adopts the company of Xilinx is key controller, have put forward a kind of the image collection system that suits area CCD. Finally, respond degree of area CCD has been tested. Experiment result shows, respond degree of area CCD is linear. The design has realized hardware eventually, is integrated as designing, have raised development efficiency.

Keywords: Area CCD, Drive timing, Response degree, FPGA

1. Introduction

Area CCD camera has gone into the fields such as the measurement with high accuracy, space remote sensing, land observation. In recent decades, with the development of space technology, CCD camera has a high accuracy measurement, in remote sensing and earth observation and other fields, and a wide range of applications. In order to make the CCD reliable performance, the driver timing is necessary for the normal work of the CCD, you need to consider the design of the digital series with the electromagnetic interference, and device delay, wires for timing signal interference factors influence of CCD performance to the best. And CCD normal work need to drive the pulse signal as many as ten road, and the driver pulse signal to keep strict between the logic and phase relationship, especially the signal in the edge of the timing relationships of the state is very important(Wu Q., et al., 2010; Xu X. Z., et al., 2004). And driving circuit for CCD provides the required is temporal logic and related voltage signal and its performance directly affect the quality of the output signal CCD, so the development of the driving circuit becomes more important.

According to the structural characteristic of area CCD, this paper have put forward a kind of the image collection system that suits area CCD, especially the design of driving circuit with high integrated degree.

2. The Area CCD Structure and Image Acquisition System

2.1 The Area CCD Structure

This paper with frame transfer area CCD is example, its internal structure such as Figure 1. To raise frame frequency the inside of frame transfer area CCD divide into the image district and the storage district, electric charge that the image district catches have been shifted the storage district after, can become picture continuously, this kind of structure of frame transfer area CCD have raised the transfer efficiency of electric

charge, suit in high speed clock carry out the transfer of electric charge (Han C. Y., 2010; Qi C., et al., 2009; Ran F., et al., 2009).

2.2 The Image Acquisition System for Area CCD

Image acquisition system represents mainly by the CCD video signal, put the processor, core controller FPGA, high-speed image acquisition card and image store and display (Shang X. S., et al., 2009; Jin L. X., et al., 2008) of its composition and data flow graph as shown in Figure 2.

3. Analysis and Simulation for Driving Signal Timing

In the ISE8.2 Xilinx company development software, the use of VHDL FPGA internal function module describing the top-down development method, and realize the high-level complex logic design, make logical relationship is very clear and reduce the logic of the complexity of the design, so as to realize the hardware design of the software. FPGA produce CCD charge transfer needs the most basic drive signal, including vertical signal (PV1, PV3 and PVTG PV2,) and level signal (PH1, PH2, PH3, PRG and PSG). CCD driver signal is divided into five categories, for a total of 132. The external active crystal clock up for input, after points and count get CCD frequency the necessary basic drive signal timing, will all drive signal timing integration in a module describe, can change the value of the counter, and convenient to change the frequency of the signal timing and occupies empties compared each signal timing and the phase relationship between.

The design process is the external input clock signal frequency have 10 MHz for division of signal timing PH level, and the PH cycle count, calculate transfer a line like the time needed for image element, because each line of the effective image element before and after eight optical dark image element, so a line of output at least 8 + 4080 for time + 8 = 4096 PH, and because the same level of the shift register two port and output, so the output a line of $2048 as time need a PH. Also, with a line of time is the cycle of PV count, calculates the transfer of a frame as the time needed for the image element, with each frame effective image element done each have 8 line up and down optical dark image element, so a frame like the output of at least $4081 for 8 + time + 8 = 4097 line, and because there are two levels of the shift register can also output, the output 2048 line, another output 2049 line, so the output of a frame like image element time need at least 2049 line.

Through the ModelSim SE simulation software of horizontal and vertical signal timing of testing, Figure 3 for level signal timing simulation results. Figure 4 for vertical signal timing simulation results. The simulation results, the signal of the representative in signal label behind the position of the CCD, ul representative part, ur representative at the left upper part, ll representative left-down part, on behalf of the right lower part, lr representatives up half part, low representative of the second half. Trig in trigger for timing signal, low level represents mechanical shutter open, high level representatives mechanical shutter closed, closed which produce a frame drive signal timing, remove all born light charge, namely the acquisition of a frame of image information.

4. The Experimental Results

Measured with an oscilloscope CCD output signal as shown in Figure 6 shows in the photo, high level corresponding RG video signal reset CCD simulation level.

First of all, all the power supply voltage and CCD detection signal voltage and timing driver, if the normal and to the top CCD, with an oscilloscope measurement output analog video signal CCD, Figure 5 for driving signal Φ RG, Φ SG and corresponding pixel CCD simulation output signal waveform, including CCD analog signal including reset level, reference level, video level three parts, the real video signal voltage reference level and video level for the difference in value between. In the fully exposure cases, CCD the maximum output video saturation voltage for 1 V, meet performance index.

The results of calibration, by fitting the response of the degrees curve get as shown in Figure 6, Figure 7 and Figure 8 below. As can be seen from the Figure 4 quadrant of the response linear degrees are all very good, linear fitting credibility reached 0.9993 (Liu Y. X., et al., 2003; Wang J., et al., 2005), it shows that the area CCD driver circuit to work normally. Among them, for the image y-coordinate of grey value, because the acquisition of the digital image said for eight, so the image gray level to 0~255, radiation intensity of illumination for the abscissa denotes (W/m^2).

5. Conclusion

According to the structural characteristic of area CCD, this paper has designed a kind of high integrated degree drive circuit and put forward a kind of the image collection system that suits area CCD. Verify through testing, respond degree of area CCD is linear. The design has realized hardware eventually, is integrated as designing, have raised development efficiency.

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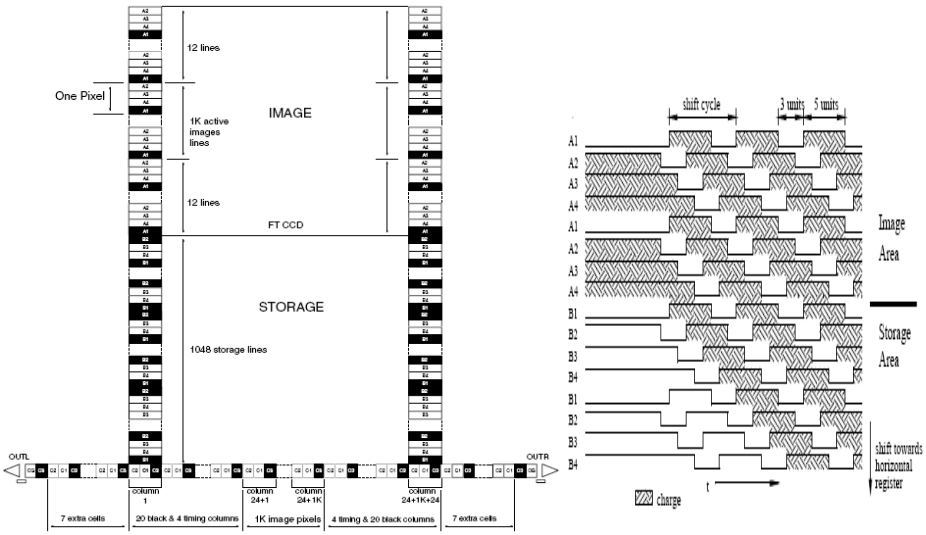


Figure 1. Frame transferred area CCD structure

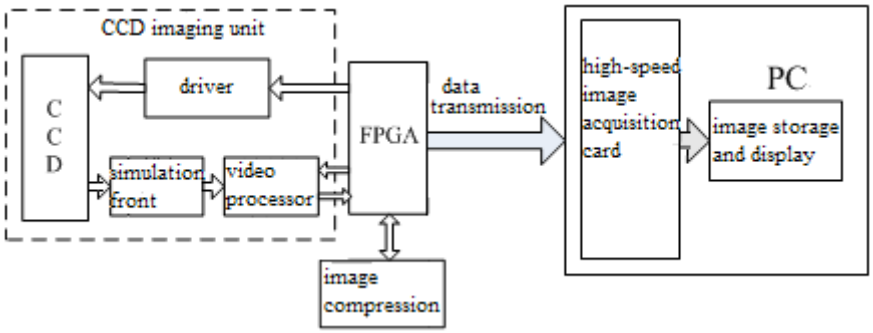


Figure 2. The composition of the area CCD image collection scheme

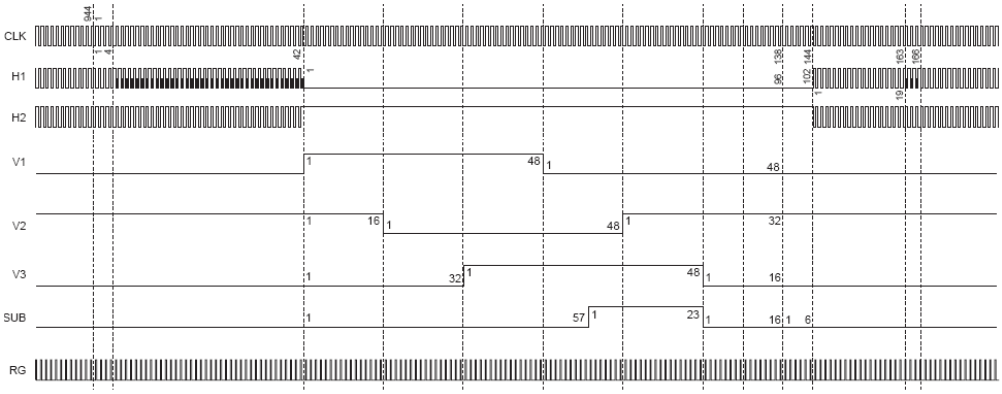


Figure 3. The sequential emulation of horizontal signal

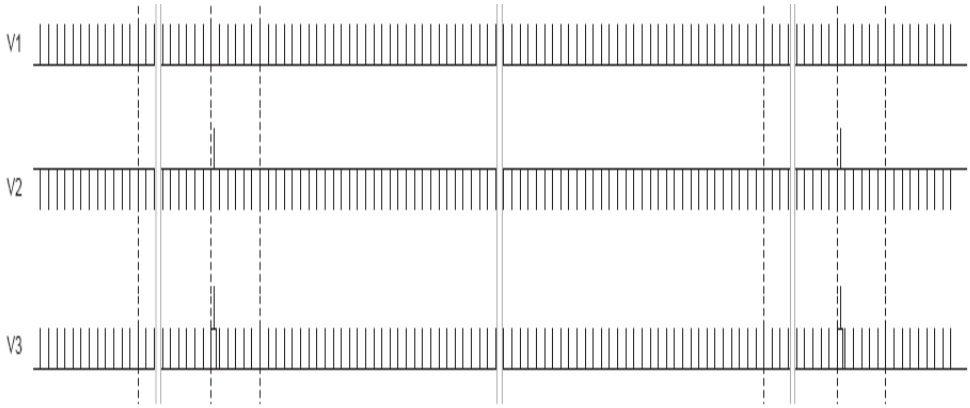
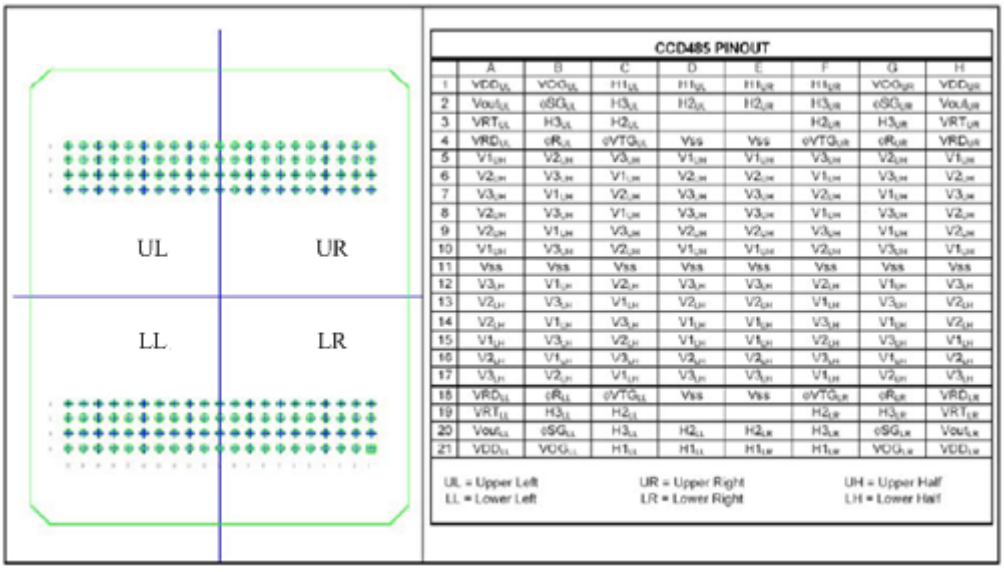


Figure 4. The sequential emulation of vertical signal



CCD485 PINOUT

	A	B	C	D	E	F	G	H
1	VDD_{UL}	VOG_{UL}	$H1_{UL}$	$H1_{UL}$	$H1_{UR}$	$H1_{UR}$	VOG_{UR}	VDD_{UR}
2	$Vout_{UL}$	ϕSG_{UL}	$H3_{UL}$	$H2_{UL}$	$H2_{UR}$	$H3_{UR}$	ϕSG_{UR}	$Vout_{UR}$
3	VRT_{UL}	$H3_{UL}$	$H2_{UL}$			$H2_{UR}$	$H3_{UR}$	VRT_{UR}
4	VRD_{UL}	ϕR_{UL}	ϕVTG_{UL}	Vss	Vss	ϕVTG_{UR}	ϕR_{UR}	VRD_{UR}
5	$V1_{UH}$	$V2_{UH}$	$V3_{UH}$	$V1_{UH}$	$V1_{UH}$	$V3_{UH}$	$V2_{UH}$	$V1_{UH}$
6	$V2_{UH}$	$V3_{UH}$	$V1_{UH}$	$V2_{UH}$	$V2_{UH}$	$V1_{UH}$	$V3_{UH}$	$V2_{UH}$
7	$V3_{UH}$	$V1_{UH}$	$V2_{UH}$	$V3_{UH}$	$V3_{UH}$	$V2_{UH}$	$V1_{UH}$	$V3_{UH}$
8	$V2_{UH}$	$V3_{UH}$	$V1_{UH}$	$V3_{UH}$	$V3_{UH}$	$V1_{UH}$	$V3_{UH}$	$V2_{UH}$
9	$V2_{UH}$	$V1_{UH}$	$V3_{UH}$	$V2_{UH}$	$V2_{UH}$	$V3_{UH}$	$V1_{UH}$	$V2_{UH}$
10	$V1_{UH}$	$V3_{UH}$	$V2_{UH}$	$V1_{UH}$	$V1_{UH}$	$V2_{UH}$	$V3_{UH}$	$V1_{UH}$
11	Vss	Vss	Vss	Vss	Vss	Vss	Vss	Vss
12	$V3_{LH}$	$V1_{LH}$	$V2_{LH}$	$V3_{LH}$	$V3_{LH}$	$V2_{LH}$	$V1_{LH}$	$V3_{LH}$
13	$V2_{LH}$	$V3_{LH}$	$V1_{LH}$	$V2_{LH}$	$V2_{LH}$	$V1_{LH}$	$V3_{LH}$	$V2_{LH}$
14	$V2_{LH}$	$V1_{LH}$	$V3_{LH}$	$V1_{LH}$	$V1_{LH}$	$V3_{LH}$	$V1_{LH}$	$V2_{LH}$
15	$V1_{LH}$	$V3_{LH}$	$V2_{LH}$	$V1_{LH}$	$V1_{LH}$	$V2_{LH}$	$V3_{LH}$	$V1_{LH}$
16	$V2_{LH}$	$V1_{LH}$	$V3_{LH}$	$V2_{LH}$	$V2_{LH}$	$V3_{LH}$	$V1_{LH}$	$V2_{LH}$
17	$V3_{LH}$	$V2_{LH}$	$V1_{LH}$	$V3_{LH}$	$V3_{LH}$	$V1_{LH}$	$V2_{LH}$	$V3_{LH}$
18	VRD_{LL}	ϕR_{LL}	ϕVTG_{LL}	Vss	Vss	ϕVTG_{LR}	ϕR_{LR}	VRD_{LR}
19	VRT_{LL}	$H3_{LL}$	$H2_{LL}$			$H2_{LR}$	$H3_{LR}$	VRT_{LR}
20	$Vout_{LL}$	ϕSG_{LL}	$H3_{LL}$	$H2_{LL}$	$H2_{LR}$	$H3_{LR}$	ϕSG_{LR}	$Vout_{LR}$
21	VDD_{LL}	VOG_{LL}	$H1_{LL}$	$H1_{LL}$	$H1_{LR}$	$H1_{LR}$	VOG_{LR}	VDD_{LR}

UL = Upper Left UR = Upper Right UH = Upper Half
LL = Lower Left LR = Lower Right LH = Lower Half

Figure 5. Drive signal distribution

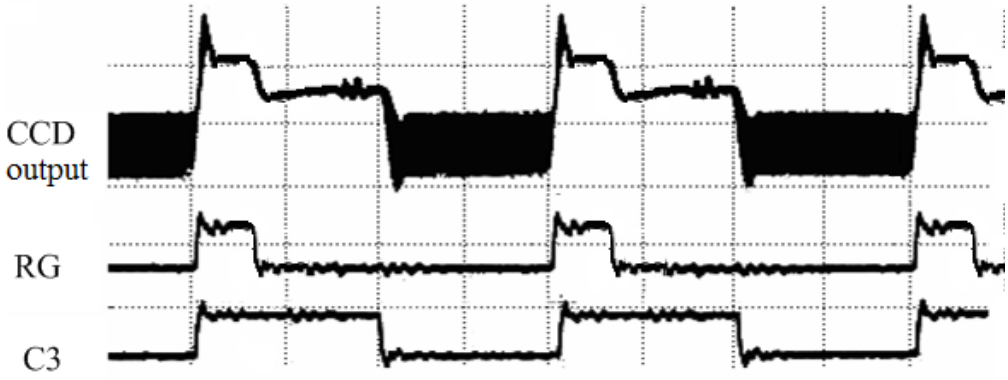


Figure 6. The driving signal sequence 1 of area CCD

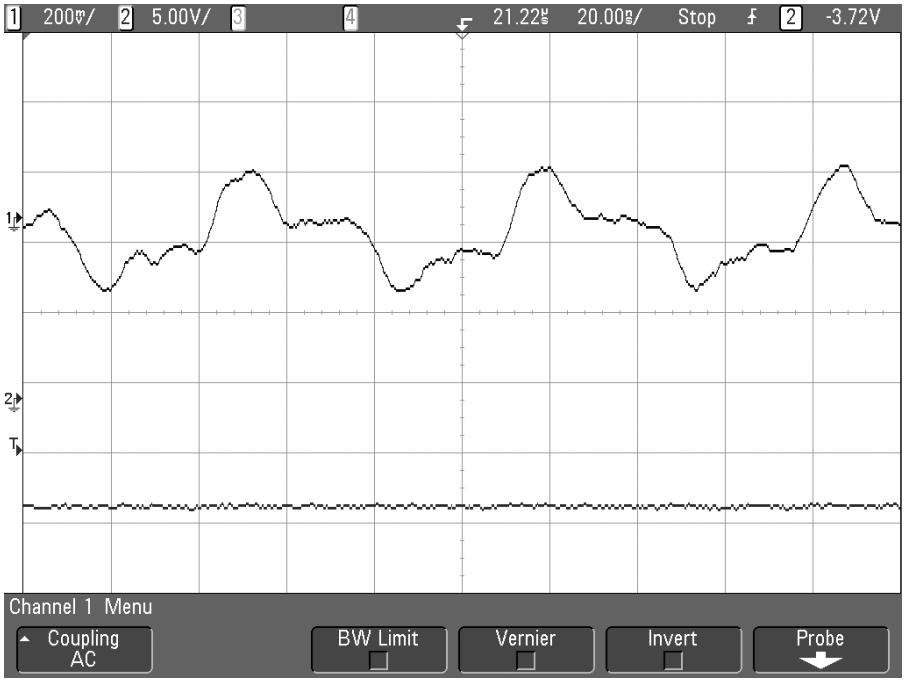


Figure 7. The driving signal sequence 2 of area CCD

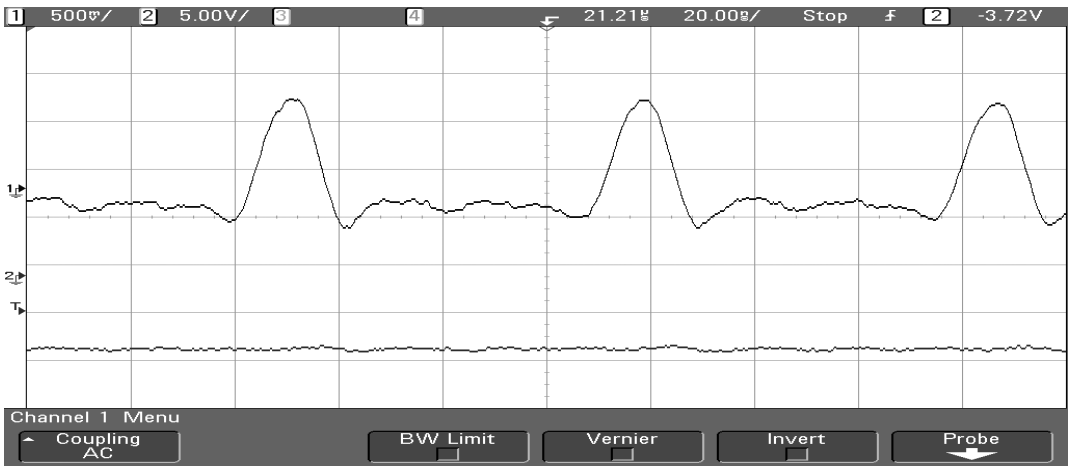


Figure 8. The driving signal sequence 3 of area CCD

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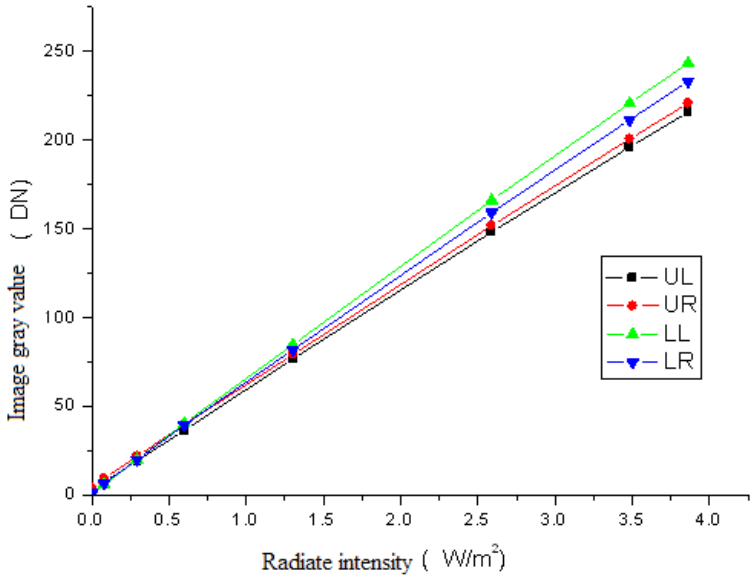

Figure 9. The response degree curve of of the 4 quadrant of area CCD

Area ccd four quadrant of the response curve fitting for formula

Upper left (UL) quadrant: $\overline{X(\varphi_k)} = 55.363 \cdot \varphi_k + 3.489$， $k = 1,2,\cdots 8$；

Upper right (UR) quadrant: $\overline{X(\varphi_k)} = 56.065 \cdot \varphi_k + 5.503$， $k = 1,2,\cdots 8$；

Left lower (LL) quadrant: $\overline{X(\varphi_k)} = 62.958 \cdot \varphi_k + 2.731$， $k = 1,2,\cdots 8$；

Right lower (LL) quadrant: $\overline{X(\varphi_k)} = 60.002 \cdot \varphi_k + 2.665$， $k = 1,2,\cdots 8$