

Porous Layers Preparation for Solar Cells by Using Effect Etching Process

Mohammed S.Mahmoud

Faculty of Engineering, University Of Malaya, Kuala Lumpur, Malaysia

Ali L. Abed

School of Applied Science, University of Technology, Baghdad –Iraq

Mohammad H. H

Center of Training and Work Shop Center, University of Technology, Baghdad -Iraq

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Abstract

Recently, nanometer size semiconductors have been a topic of great interest. Electrochemical and /or chemical etches of silicon produce P-Si layers have a strong link between the details of processing and the optical and electronic properties of the resulting structure. This paper focuses on investigation different affecting parameters on the surface morphology, etching rate, electrical properties. Good electrical properties (low resistivity and high passing current) achieved by electrochemical etching when appropriate etching current density and short etching time of 10 min.

Keywords: Nanometer size semiconductors, Solar cells, Effect etching process

1. Introduction

Nowadays, Solar cell technologies are an attractive option for clean and renewable energy generation in the form of electricity. Several technologies have been developed since 1950s and many of them now reached to commercialization stage. However, photovoltaic (PV) solar cells are not economically efficient yet when compared to the ordinary grid power used nowadays. P-Si is not a new material. It was first reported over 40 years ago during electropolishing of Si in aqueous HF acid observed by Uhler, but was basically a nuisance at that time, since it supposed to be a Si sub oxide (D. P. Lasher, B. A. Decraff, and B. H. Augustin. 2000)(J. T. Frederksen, P. G. Mecher, and E. Veje. 1998). P-Si are widely used in solar cell applications because of the increase of the absorption coefficient with its energy and due to the simplicity of the fabrication so, solar cell incorporating P-Si can be achieved at low cost (S. Bastide, A. Albu-Yaron, S. Strenlke, and C. Lévy-Clément. 1999). The most commonly P-Si production technique used is the electrochemical etching in which biasing is required to initiate the chemical reaction which produce a well-controlled photoemission characteristics of porous layer.

Recent studies (K.W. Kolasinski, A. Wallner, R. Neaendorf, C. X. Pederson, and R. E. Palmer. 2001)(S. Stolyarova, A. El-Bahar, and Y. Nemirovsky. 2000) have shown that certain electrochemical (EC) etching of Si produce a microporous material (P-Si) Porous silicon is quickly becoming an increasingly important and versatile electronic material in today's fabrication technology (R. L. Smith, and S. D. Collins. 1992). P-Si is a complex network of pores separated by thin columns and contains nano-meter sized Si crystallites. The relationship between fabrication conditions and the structural and electronic properties of P-Si was examined extensively in subsequent work(V. Lehmann, and U. Gosele. 1991). The current density, HF acid concentration, etching time, presence or absence of illumination during etching and, in particular, the doping type and resistivity of the Si influence the morphology of porous layer(R. T. Collins, P. M. Fauchet, and M. A. Tisler. 1997).

The most common P-Si preparation method which transforms silicon to large-surface area material using constant current densities in the range of 1-300 mA/cm² in aqueous HF solutions (Z. C. Feng and R. Tsu, 1994). Many researches have established the decrease of the density of the P-Si layer at increasing value of the anodic current. The Si surface serves as the anode, while the cathode is made of platinum or any conducting

HF-resistant material. The cell body itself is made of highly acid-resistant polymer such as plastic or Teflon (V. Lehmann, and U. Gosele. 1991). HF is diluted in an aqueous solution (ethanol and DI water) with up to 50% of HF. In fact, ethanoic solutions infiltrate the pores.

Nansheng et al. (Zh. Nansheng, M. Zhongquan, Zh. Chengyue and H. Bo. 2009) formed PS layer by electrochemical etching in emitter layer of solar cell with very low reflectivity was obtained. The morphology and reflectivity of PS layer are easily modulated by controlling the electrochemical condition (i.e. the current density and etching time). It has been shown that the reflectivity of approximately 1.42% in the range 380-1100nm is realized by using optimized condition.

This paper focuses on investigation of the effect etching process to fabricate nanostructure solar cell by electrochemical technique with different current density. Moreover, effects of the effective parameters on the surface morphology and the device parameters can be used to determine the optimization preparation condition on the solar cell conversion efficiency. The main results are in terms of minimization of the reflection losses and reduction of the density of the surface states. More recently, the effects of using a PS layer on the front surface of a crystalline Si solar cell have been extensively investigated (O. V. Brodovoy, V. A. Skryshevsky and V. A. Brodovoy, 2006). The minimization of the optical losses has been obtained by electrochemically etching a 10 μ m thick porous layer on Si substrates and treating it in a HF-based solution. In this manner, the achieved effect is comparable to the best AR coating obtained depositing a double layer (ZnS+MgF₂) on a pre-textured Si surface. Specifically the integrated reflectance changes from 1.6% to 3.4% in the wavelength from 400 to 900nm. However, when PS is formed on polycrystalline Si, the integrated reflectance in the 300-900 nm spectral region is around 10%. In the same study, porous Si has been formed on the front surface of a point-contact Si solar cell to increase the total amount of the light absorbed and improve the efficiency. But all the tested cells show a degradation of the open-circuit voltage and of the short-circuit current density. The degradation of the cell performances was explained by the increased surface recombination caused by the partial removal of the very efficient front surface oxide layer (O. Nichiporuk, A. Kaminski, M. Lemiti, A. Fave, S. Litvinenko and V. Skryshevsky, 2006).

2. Experimental Setup

PS layers with various porosities were fabricated by electrochemical etching of a highly doped *p*-type <100> oriented silicon substrate with a resistivity of 0.01–0.02 Ω cm in the mixture of hydrofluoric acid and ethanol. The set-up for the electrochemical etching consists of power supply as a current source, ammeter and HF acid in plastic container. Fig. (1) shows a schematic diagram of the ECE set-up, crystalline silicon samples (c-Si) was cut into small pieces with dimensions of (1x2 cm). The thicknesses of the wafers were nearly 500 μ m. The samples were cleaned, then rinsed and mounted on a Teflon cell in such a way that current could only pass between the faced surfaces of the silicon substrate and the platinum. The silicon was mounted as an anode and completes the electrical by putting a platinum mesh as a cathode in a parallel way to achieve homogeneous layers of P-Si. The HF acid should be diluted with ethanol to minimize the hydrogen bubbles during the etching which starts within a few minutes. The process was carried out at acid concentration (40%), different etching times (10-60min.), and different current densities (10-120mA/cm²). All these requirements were considered as effective parameters in the ECE process. In this work the current density passes through only the immersed area of the two electrodes to form a layer of P-Si. After that, samples were kept in a plastic container of ethanol to prevent oxidation of P-Si layers. The thicknesses of the porous layers determined with an optical microscope were in the range of 8–34 μ m. The changes in surface morphology of three different PS samples were investigated by using a scanning electron microscope (SEM) (EVO550, Carl Zeiss).

The current from the current generator was passed through the etchant solution. As the current moves from anode to cathode, it provides a flow to ions in the solution toward the sample. The anodic ions release electrons when they reach the surface of the substrate across the solution. The *p*-doped sample pushes these electrons into its holes, depleted and combined with neighboring holes. It eventually creates an etched area around the pattern. Each test was initiated by activating the time counter and the current source. The etched depth was varied by the duration of etching.

3. Result and Discussion

The most important applications of porous silicon (PS) devices consisting silicon nanostructures is optoelectronic and specifically solar cells. Porous silicon was produced by electrochemical etching process with different anodization conditions were include current density and etching time at HF acid of 40 % concentration to control the electrical properties and surface morphology of the prepared devices. These properties strongly depend on the structure characteristics of the formed PS layer, SEM analysis indicates that etching times ranging

from (10 - 60 min) yield a progression of P-Si layers morphologies. In general, etching times less than approximately 20 min yield a ridged porous structure as shown in Fig. 1a. The porous morphology is homogeneous across the entire wafer surface, although occasional pockets of varying degrees of porosity are observed. Longer etch times (≈ 60 min) yield different morphologies, porosity results that is restricted to the near-surface region. morphology results. As etching process proceeds, extra holes reach the surface leading for further dissolving of the Si, and with more time the carriers will confined in the thin column leading for dissolve these columns and excessive etching take place until the carriers rearrange again on the whole surface and initiate a new layer as show in (Fig. 1b). The key difference between the morphologies obtained at short and long times appears in the lateral etching. At shorter etch times the etching occurs inhomogeneously in the plane, but is largely directed perpendicular to the original surface. At longer times the etching develops more lateral structure with etching proceeding to undercut some of the structures confined to the surface

The effect of the etching time also studied and the optimum layer thickness could be obtained at 60 minutes. As the etching time proceeds, excessive etching leads to decrease the P-Si layer thickness since longer etching time leads to remove the porous layer formed at early stage.

The porosity is defined as the fraction of void within the PS layer. which is strongly dependant on the anodization conditions. From fig. (3), it is clear that the effect of etching time with the porosity of P-Si layer is linear function when the etching time is increased some columns disappeared due to excessive etching was observed. Average size of columns decreased with increasing etching time (10min to 50min) but the porosity increased with increasing etching time.

The effect of current density on the PS formation was examined. the current density plays a significant role in controlling the porous morphology which is considered as an important feature for nanostructured solar cells. For small current density of 15mA/cm^2 , the surface of c-Si is converted into relatively rough surface but the porous layer has small thickness. When the current density increased, new structure (column) would appear due to more effective holes accumulation. Generally, increasing current density (50mA/cm^2) leads to an increase in the thickness of porous layer and the pillar width to about $24\mu\text{m}$. Increasing the etching current density leads to a reduction of pore diameters.

High current density increases the etching rate and the porous layer in the thickness direction leaving the pore diameter slightly changed. As a result, the etching rate could be estimated as a function of current density and etching time. The etching rate of electrochemical etching process has attracted a great attention since it describes the etching process speed. The etching rate depends on the formation parameters and governed by the diffusion rate and drift velocities of holes to the surface. One can easily recognize that the etching rate increases exponentially with the current density for P-Si layers were prepared with HF acid of 40 % concentration for 60 minutes in Fig. (4), And this could be explained as follows; When the current density increased, the hole accumulation becomes larger and then, holes consummation will be faster since the responsible chemical reaction depends strongly on the supplied holes.

The Electrical Properties the nanostructured solar cells prepared at different conditions are presented in this paper . In general, $J-V$ characteristics was studied to examine its influence on the electrical properties the forward bias current is originated from the transport of majority charge carriers. As the voltage is applied, the majority charge carriers are injected, which in turn causes to lower the built-in potential and decrease the width of depletion region, then the product of majority and minority charge carriers concentrations is larger than the squared intrinsic carriers concentration ($n_i^2 < np$). The current is responsible to accumulate holes while the consumption is almost slow. At low etching current densities, the accumulation process is very slow and the thickness of the formed porous layer is too small, i.e., the current flowing through the cell is small. Increasing the etching current density will increase the density of the accumulated holes (collected) on the surface consequently, a current is generated to get the balance back, This current is known as "recombination current" and occurs at low voltages only.

4. Conclusions

Different preparation parameters are affecting the surface morphology of the nanostructured solar cell. Increase of current density results in more porous silicon surface layer and the corresponding pores are deeper. At low current density chemical etching prevails and pores shape is more complex and branched, Geometry of the pores and etching anisotropy changes, when different current density is used. The optoelectronic properties could determine the optimum preparation conditions which give higher conversion efficiency of the device. In addition the small etching time (10min) and low current density are preferable to obtain porous layers of good electrical properties and at very low current density (10mA/cm^2) of the electrochemical etching, the conversion efficiency

increases when it's compared with that of the ordinary solar cell. Finally, the surface area increases with increasing the preparation current density for p-type silicon

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Table 1.

Preparation Time (min)	P-Si thickness (μm)
10	8
20	12
30	20
60	34

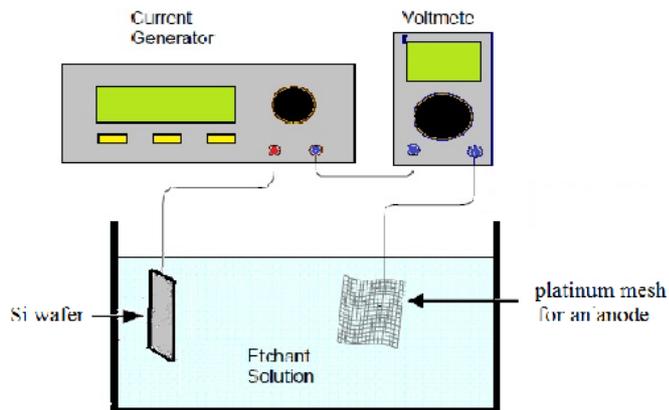


Figure 1. The electrochemical etching setup

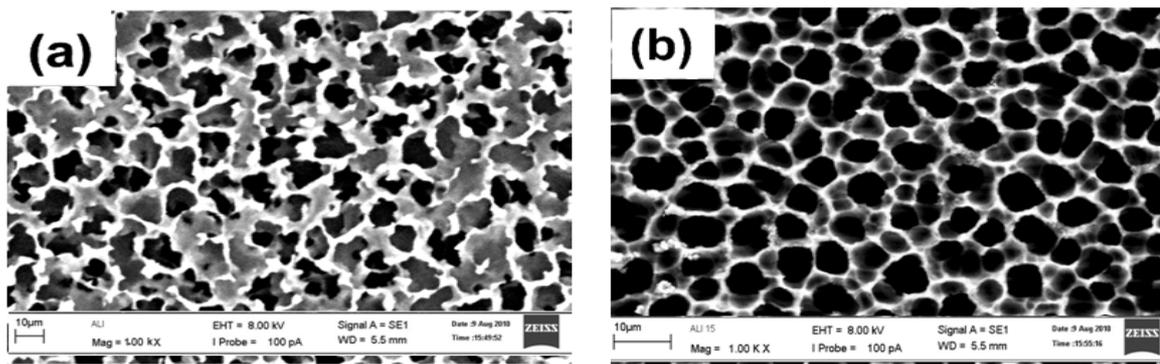


Figure 2. SEM images of silicon surface etched with etching times (a) 10 minutes, (b) 50 minutes

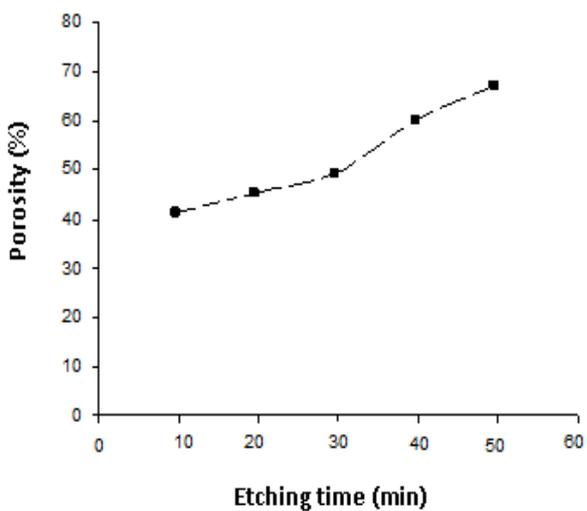


Figure 3. The porosity as a function of etching time

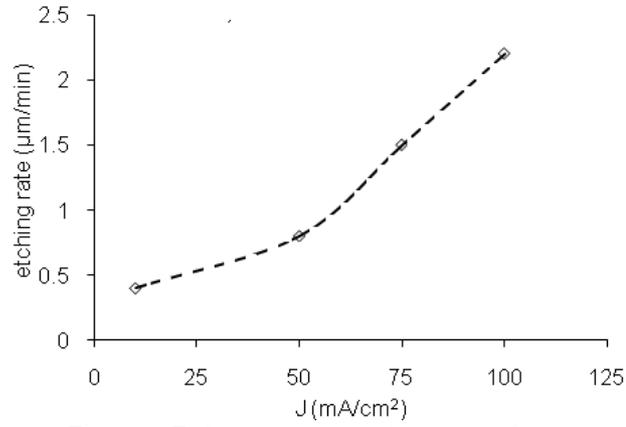


Figure 4. Etching rate versus the current density

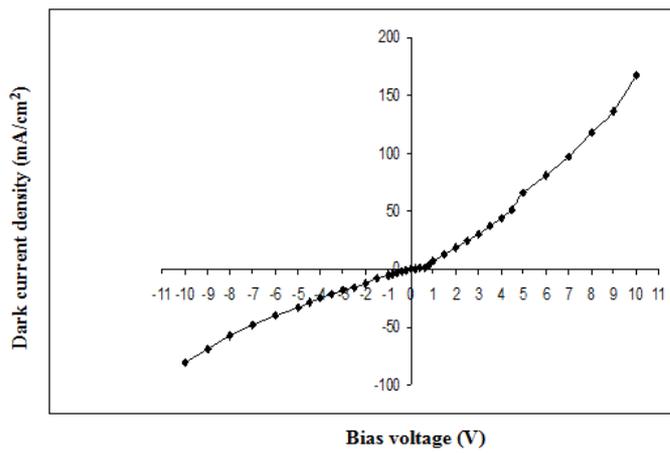


Figure 5. The J-V characteristics of solar cells contain P-Si layers prepared at an etching time 20 min