Design of Time Division MUX and DEMUX for Large Optical Transceiver

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Abstract

The working principle of large optical transceiver is introduced in this article, and the time division MUX and the time division DEMUX are designed by the online system programmable technology and the FPGA (Field Programmable Logic Array), including hardware design, software design, and testing. The transmitting design and the receiving design method of time division MUX are introduced in detail, and a kind of time division MUX method based on synchronic control character is designed to realize the reliable transmission of VGA signals, PAL signals, voice signals, digital IO, USB data, and network signals, which is helpful and practical to enhance the capacity of transmission channel and save the fiber resources.

Keywords: Optical communication, TDM (Time Division Multiplex), Large optical transceiver, FPGA

1. Introduction

At present, with the increase of transmitted information kinds and the explosive growth of data quantity, large numbers of information is transmitted by the fibers, but traditional transmission equipment could only transmit single information, for example, the video signal and the network signal could respectively occupy their own fiber, and the resources of fiber are largely wasted. The TDM technology could combine and separate different types of data, in favor of the transmission of multiple kinds of information. The application FPGA (Field Programmable Gata Array) makes the implementation of TDM more easy and reliable. With high integrated level, FPGA could complete very complex function of time sequence circuit and combinational logic circuit, being appropriate for the digital logic circuit design with high speed and high density. At present, the multiplexing mode adopted by some optical transceivers is not flexible, inducing low use ratio of channel. A method based on TDM is proposed in this article, which could flexibly process the data with different speeds, and transmit them together through the multiplexing mode, with good effect.

2. System composition

The system transmitting the information through fibers is composed by the transmission equipment and fibers, and the optical transmission equipment is used in pair, i.e. the optical transceiver. The working principle of the optical transceivers is seen in Figure 1.

3. Design principle

The system is single-module and single fiber, which can transmit one-way VGA signals, two-way video signals, two-way stereo audio, 64-way data, two-way USB data, and four-way Ethernet data.

3.1 Hardware design

VGA video interface: The AD part adopts the ADV9883 chip, 140 MHZ sampling, and 24 bits quantized data output, and the DA part adopts ADV7125 chip, and 24 bits data input.

PAL video interface: The AD part adopts the ADV7403 chip, 110 MHZ sampling, and 19 bits quantized data output, and the DA part adopts ADV7392 chip, and 24 bits data input.

Audio interface: The AD part adopts the CS5340 chip, and the left and right sound track audio bands respectively are quantitated by 78.125 KHZ and 24bits clock with 8 bits synchronous code, and two track audio bands with 64 bits compose the data output of 5 Mbit/s. And the DA part adopts CS4344 chip, and restores the left and right sound track audio bands.

Data interface: Adopt MAX3232 chip, and completes the switch of the RS232 data interface level and the TTL level.

Network interface: Adopt KS8695 chip.

USB interface: Adopt US2514 chip.

FPGA: Adopt XC5VFX70T-2FF665I chip. The concrete works are completed by the software design.

3.2 Software design

The whole software design is implemented on the Xilinx development platform ISE12.4 by the VHDL language programming.

3.2.1 Collection of the data from various interfaces by FPGA

The data acquisition is seen in Table 1.

3.2.2 MUX and DEMUX

MUX and DEMUX are emphases of the design in this article. The digital MUX method includes the positional MUX, the byte-MUX, and the frame MUX according to the length of each channel signal. The positional MUX requires simple equipment, small storage capacity, and is easy to be implemented, but it requires that the code rates of each set of equipment are same. The frame-MUX doesn't destroy the structure of former frames, in favor of exchange.

According to the relationships among various branch signal clocks, the TDM can be divided into the synchronous multiplexing, the asynchronous multiplexing, and the quasi-synchronous multiplexing. If the clocks of various branch signals don't come from same one clock source, and various signals have no the synchronous relationship, that is called as the asynchronous multiplexing. For asynchronous multiplexing, the asynchronous FIFO should be used to synchronize the asynchronous data, or else, the system will enter into the metastable state. With respect to the synchronous multiplexing technology, the quasi-synchronous multiplexing increases the code rate adjusting function and the code rate recovering function. The design in this article adopts the synchronous multiplexing, and comparing with above two modes, the system is not easy to enter into the metastable state, and has not the part of code rate processing, so the system will be more reliable and stable.

The clocks used by various branch signals in the synchronous multiplexing mode come from one clock, and from Table 1, there are three kinds of multiplexing data rate in this system which could not depend on the multiplexing arbitration one time, so the secondary multiplexing arbitration is proposed in this design. It processes the data with different rates, and combines them flexibly, and ensures the transmission of data with different speeds, and largely enhances the using rate of channel. The multiplexing principle is seen in Figure 2.

In each time, 8 bits data are multiplexed, and the former seven bits are valid data, and the eighth bit is the zone bit, used for the branching synchronization. The concrete multiplexing process can be described as follows.

(1) Processing of networkdata

Implement the series-parallel conversion for the network data by the interior shift register in FPGA, and convert five 25 Mbit/s network data into twenty-five 5 Mbit/s data.

(2) Once multiple-connection

Use the rising edge of 15 MH clock to trigger the counter with the module of 3. The once multiplexing is to multiplex the data of 5 Mbit/s, and the multiplexed data are the data of 15 Mbit/s, and the multiplexing includes two groups (Seen in Figure 3).

(3) Secondary multiplexing

Use the rising edge of 60 MH clock to trigger the counter with the module of 4. The secondary multiplexing is to multiplex the data of 15 Mbit/s, and the multiplexed data are the data of 60 Mbit/s, and the concrete multiplexing process is seen in Figure 4.

3.2.3 Branching

DEMUX is the inverse process of MUX, and it could complete 12 beats under the controlof the recovering 60 MHZ clock, and control the start of the beat by the received zone bit. The recovering 60 MHZ clock signals are transmitted by the serial-parallel conversion chip, and other clock signals come from this clock. The DEMUXvideo data change in each 4-beat and the speed is 15 Mbit/s, and other data change in each 12-beat, and the speed is 5 Mbit/s. The 15 M recovering clock transmitsDEMUX the video data to the video interface, and the 5 M recovering clock respectively transmits the DEMUX audio signals and the DEMUX data to the audio

interface and the data interface. The 5 Mbit/s DEMUX network data must be processed and twenty-five 5 Mbit/s data should be restored to five 25 Mbit/s data. In FPGA, 25 MHZ recovering clock is used to read five 5 Mbit/s data in serial mode and complete the parallel-serial conversion, and transmit five 25 Mbit/s data to the network interface. The process of DEMUX is seen in Figure 5.

4. Testing

Load the compiled object files to the test board FPGA for testing. Except for the zone bit in the eighth channel in the multiplexing processing, the data in other channels are valid data, and the use rate of channel is very high (seen in Table 2).

5. Conclusions

The multiplexing mode of digital optical transceiver is studied in this article, and according to the difference among video signals, audio signals, data, and network data, the secondary multiplexing mode is adopted, which can adjust and process the data with different speeds, and the data are transmitted after the secondary multiplexing. The test result shows that the optical transceiver with this multiplexing mode has good signal index, stable performance, high channel use rate, and less fiber resources, and this new optical transceiver can be widely used in many domains such as intelligent traffic, security and prevention, and industrial monitoring.

References

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Table 1. Collection statistics of signal data

Signals	Signal quantity	Time occupied by each signal	Speed (Mbit/s)
Video	1	8	15
Audio	2	1	5
Data	8	1	5
Network	1	5	25

Table 2. Signal parameters

| Product	Video		Audio		Data		Network	
	Width	SNR/dB	Width	SNR/dB	Speed(Kbit/s)	Error rate	Work mode	Packet loss ratio
Design	50Hz~80Hz	>=67	20Hz~20KHz	>=85	0-256	<=10-9	10/100M Adaptive Ethernet	0
	50Hz~80Hz	>=65	20Hz~20KHz	>=80	0-256	<=10-9	10/100M Adaptive Ethernet	0
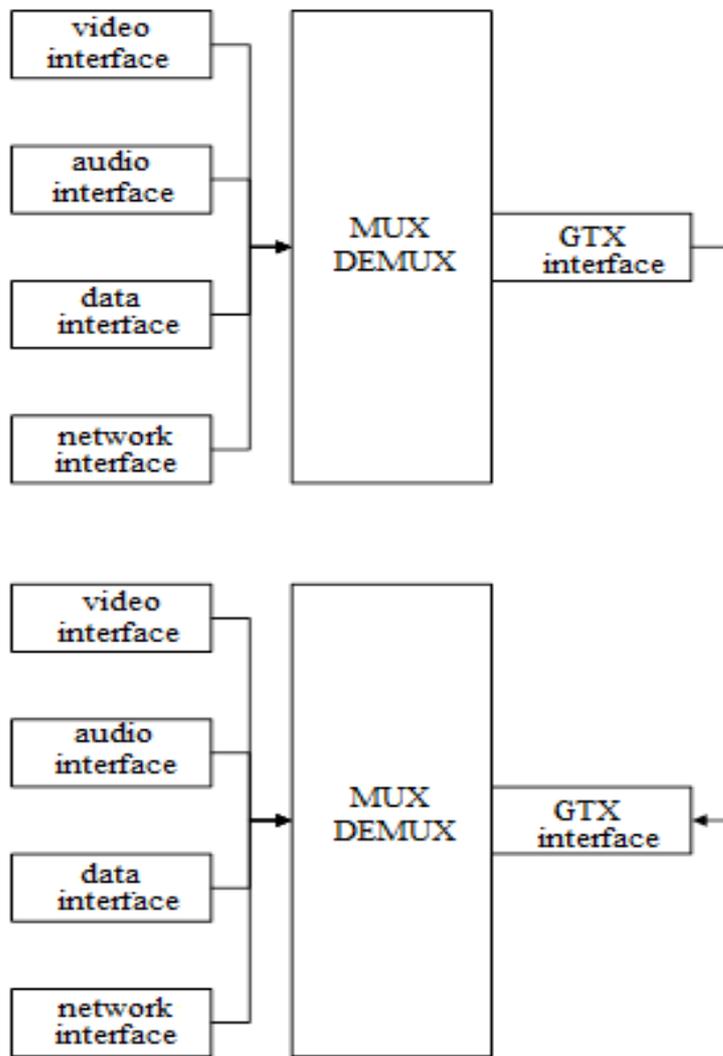
Figure 1. Working Principle of Optical Transceiver
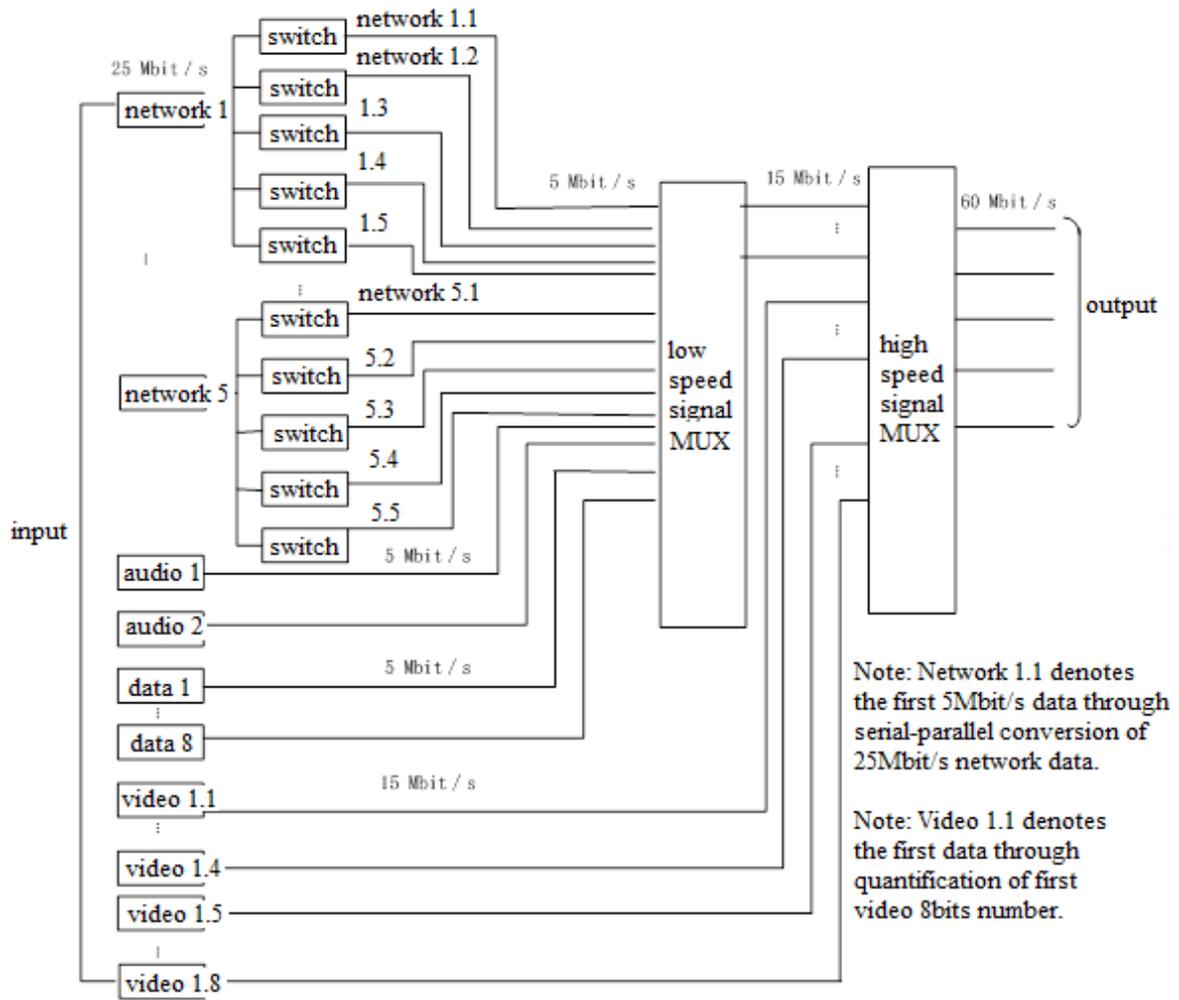
Figure 2. MUX principle
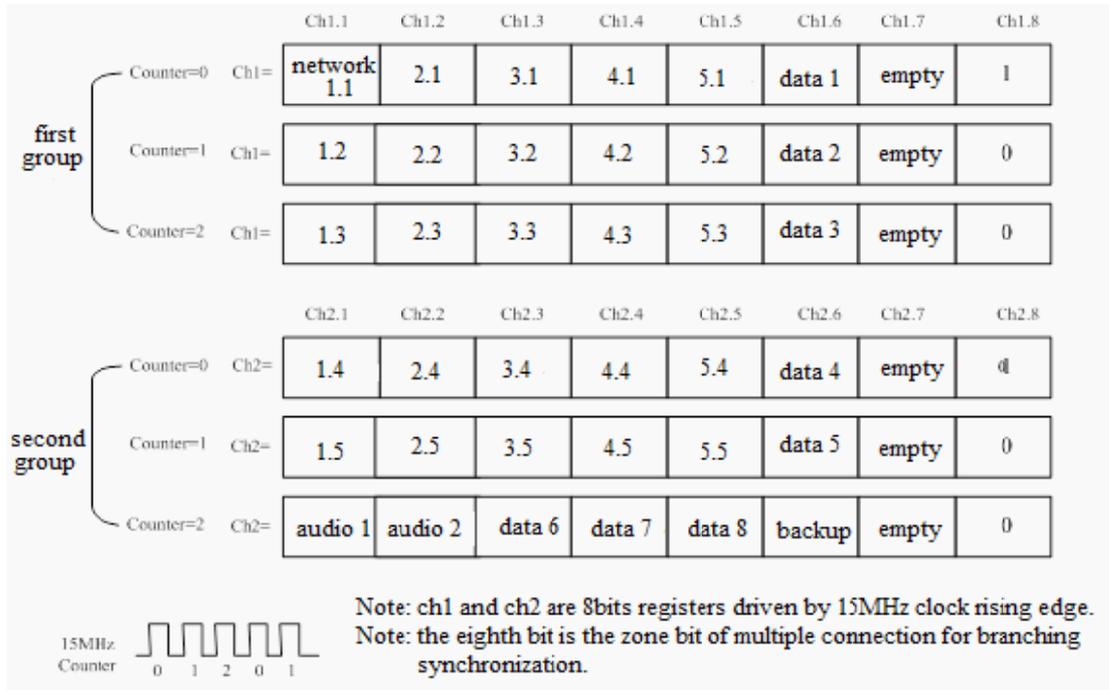
Figure 3. Process of MUX
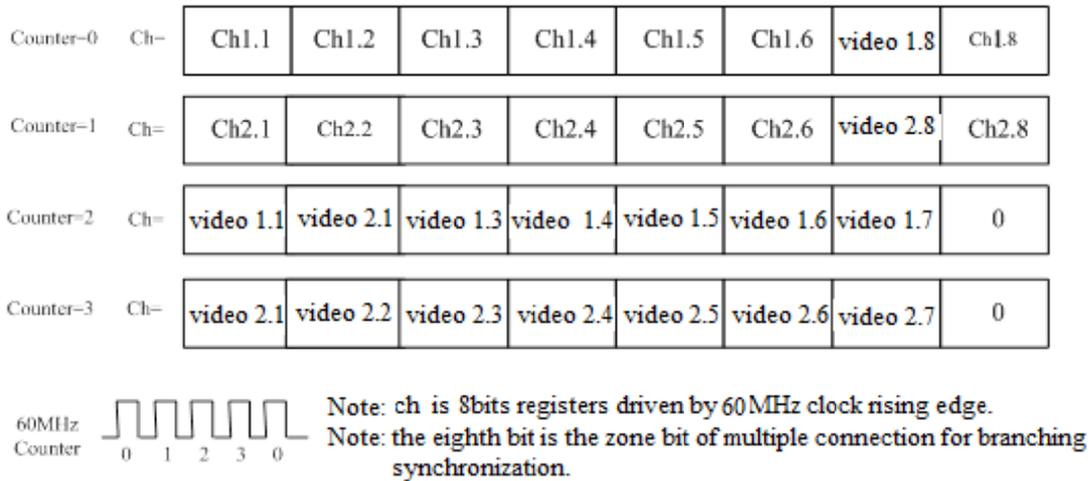
Figure 4. Process of Two MUXs

Counter	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8
1	network 1.1	network 2.1	network 3.1	network 4.1	network 5.1	data 1	video 1.8	1
2	network 1.4	network 2.4	network 3.4	network 4.4	network 5.4	data 4	video 2.8	0
3	video 1.1	video 1.2	video 1.3	video 1.4	video 1.5	video 1.6	video 1.7	0
4	video 2.1	video 2.2	video 2.3	video 2.4	video 2.5	video 2.6	video 2.7	0
5	network 1.2	network 2.2	network 3.2	network 4.2	network 5.2	data 2	video 1.8	0
6	network 1.5	network 2.5	network 3.5	network 4.5	network 5.5	data 5	video 2.8	0
7	video 1.1	video 1.2	video 1.3	video 1.4	video 1.5	video 1.6	video 1.7	0
8	video 2.1	video 2.2	video 2.3	video 2.4	video 2.5	video 2.6	video 2.7	0
9	network 1.3	network 2.3	network 3.3	network 4.3	network 5.3	data 3	video 1.8	0
10	audio 1	audio 2	data 6	data 7	data 8	backup	video 2.8	0
11	video 1.1	video 1.2	video 1.3	video 1.4	video 1.5	video 1.6	video 1.7	0
12	video 2.1	video 2.2	video 2.3	video 2.4	video 2.5	video 2.6	video 2.7	0

60MHz Counter   0 1 2 3 4 5 6 7 8 9 10 11 12 1
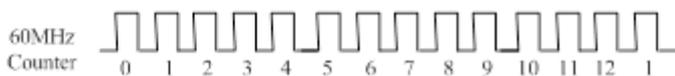
Note: counter is the counter of the ch.8 zone bit contorl initial value triggered by 60MHz clock, and when the zone bit is 1, counter = 1.

Figure 5. Process of DEMUX